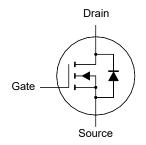
N-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 Qualified
- Low R_{DS(on)} to minimize conduction losses
- · Low capacitance to minimize driver losses
- Halogen and Antimony Free(HAF), RoHS compliant





 Source 2. Source 3. Source 4. Gate
Drain 6. Drain 7. Drain 8. Drain DFN5060 Plastic Package

Application

• Synchronous buck converter

Key Parameters

Parameter	Value	Unit		
BV _{DSS}	40	V		
Prevent Mov	3.3 @ V _{GS} = 10 V	mΩ		
R _{DS(ON)} Max	4.9 @ V _{GS} = 4.5 V	mΩ		
V _{GS(th)} typ	1.5	V		
Q _g typ	45 @ V _{GS} = 10 V	nC		

Absolute Maximum Ratings (at Ta = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _{GS}	± 20	V	
Continuous Drain Current	$T_c = 25^{\circ}C$ $T_c = 100^{\circ}C$	I _D	75 47	А
Peak Drain Current 1)		I _{DM}	420	Α
Avalanche Current		las	40	Α
Single Pulse Avalanche Energy ²⁾		E _{AS}	80	mJ
Power Dissipation	$T_c = 25^{\circ}C$ $T_c = 100^{\circ}C$	P _D	27.8 11	W
Operating Junction and Storage Temperature Rang	T _J , T _{stg}	- 55 to + 150	°C	

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	R _{eJC}	4.5	°C/W
Thermal Resistance from Junction to Ambient 3) Steady State	Reja	45	°C/W

¹⁾ Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 150°C.



 $^{^{2)}}$ Limited by $T_{J(MAX)},$ starting T_J = 25 °C, L = 0.1 mH, R_g = 25 $\Omega,\,I_D$ = 40 A, V_{GS} = 10 V.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

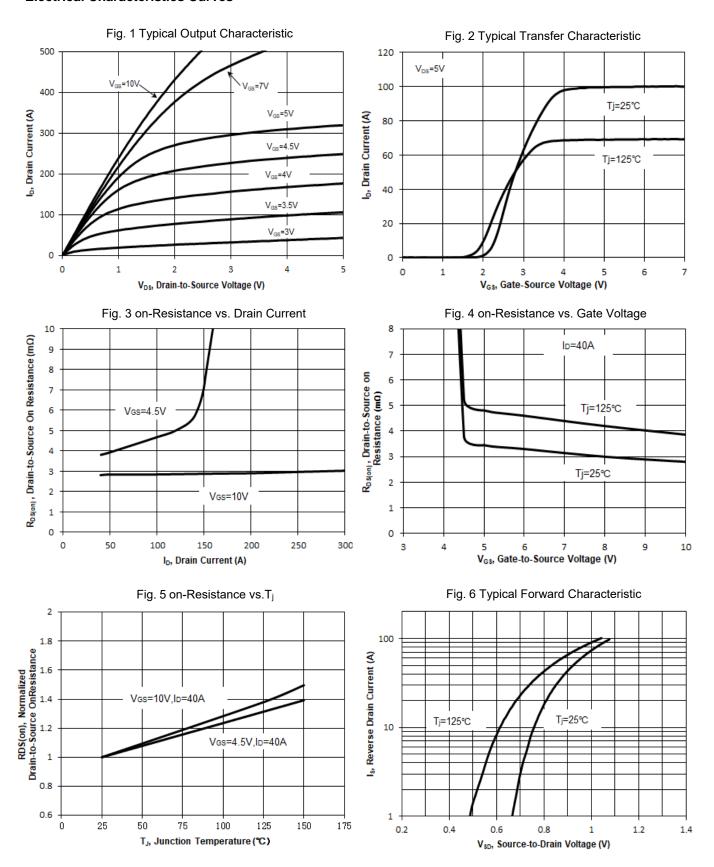
WTM504N031L-AH

Characteristics at Ta = 25°C unless otherwise specified

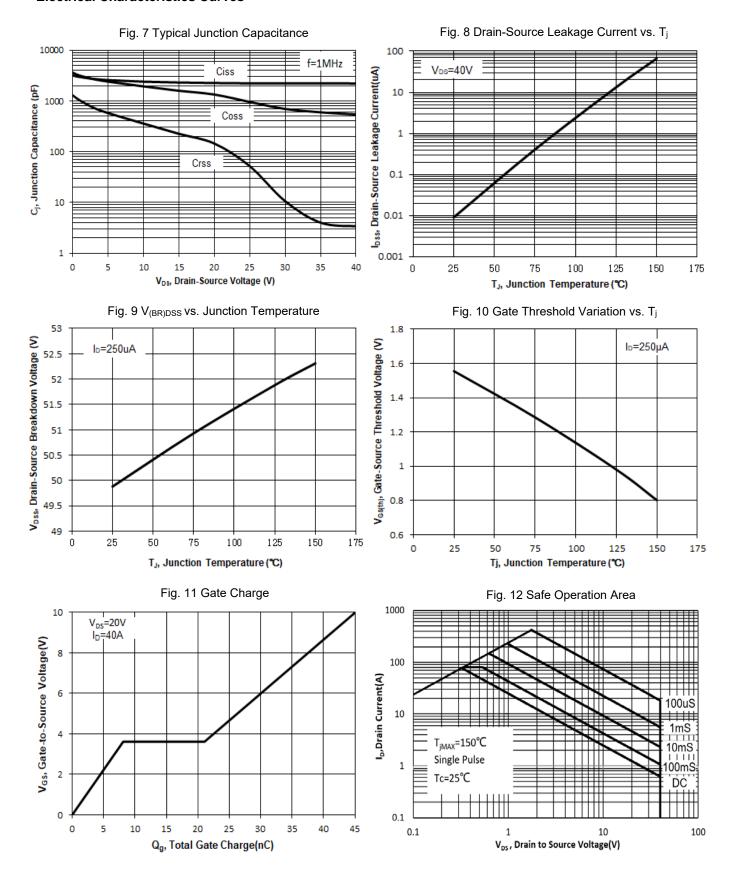
Parameter	Symbol	Min.	Тур.	Max.	Unit
STATIC PARAMETERS	1		•	•	
Drain-Source Breakdown Voltage at I _D = 250 μA	BV _{DSS}	40	-	-	V
Drain-Source Leakage Current at V _{DS} = 40 V	I _{DSS}	-	-	1	μΑ
Gate Leakage Current at V _{GS} = ± 20 V	lgss	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS} , I_D = 250 μ A	V _{GS(th)}	1.2	-	2.2	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 40 A at V_{GS} = 4.5 V, I_D = 40 A	R _{DS(on)}	- -	2.8	3.3 4.9	mΩ
DYNAMIC PARAMETERS					
Gate resistance at V _{DS} = 0 V, f = 1 MHz	Rg	-	2.2	-	Ω
Forward Transconductance at V_{DS} = 5 V, I_D = 40 A	g fs	-	25	-	S
Input Capacitance at $V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$	Ciss	-	2225	-	pF
Output Capacitance at $V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$	Coss	-	956	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$	Crss	-	52	-	pF
Gate charge total at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 10 V at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V	Qg	- -	45 23	- -	nC
Gate to Source Charge at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V	Q _{gs}	-	8	-	nC
Gate to Drain Charge at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V	Q_{gd}	-	13	-	nC
Turn-On Delay Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	t _{d(on)}	-	29	-	nS
Turn-On Rise Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	t _r	-	107	-	nS
Turn-Off Delay Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	$t_{d(off)}$	-	22	-	nS
Turn-Off Fall Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	t _f	-	37	-	nS
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $I_S = 40 \text{ A}$, $V_{GS} = 0 \text{ V}$	V _{SD}	-	-	1.2	V
Body-Diode Continuous Current	ls	-	-	75	Α
Body-Diode Continuous Current, Pulsed	Ism		_	420	Α
Body Diode Reverse Recovery Time at I_S = 40 A, di/dt = 100 A / μ s	t _{rr}	-	30	-	nS
Body Diode Reverse Recovery Charge at I_S = 40 A, di/dt = 100 A / μ s	Qrr	-	17	-	nC



Electrical Characteristics Curves



Electrical Characteristics Curves





Electrical Characteristics Curves

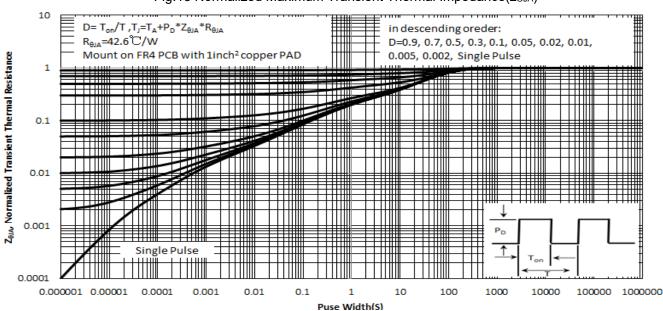
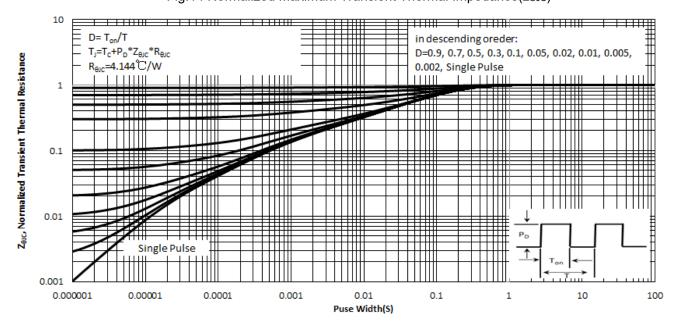


Fig.13 Normalized Maximum Transient Thermal Impedance(zeja)



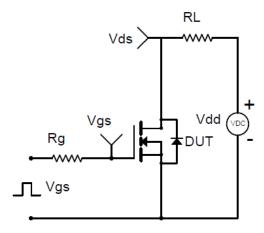




WTM504N031L-AH

Test Circuits

Fig.1-1 Switching times test circuit



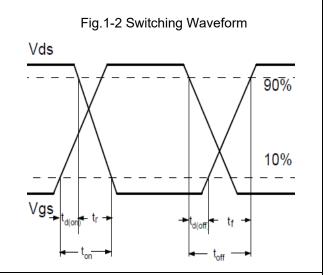


Fig.2-1 Gate charge test circuit

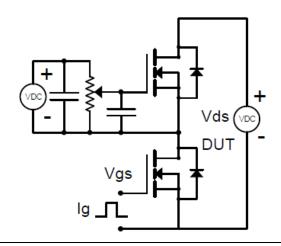


Fig.2-2 Gate charge waveform

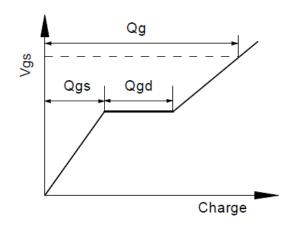


Fig.3-1 Avalanche test circuit

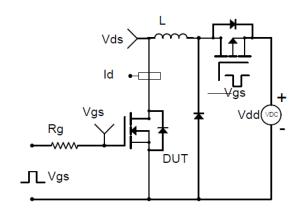
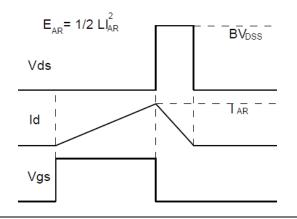


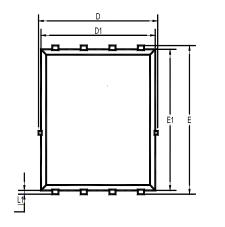
Fig.3-2 Avalanche waveform

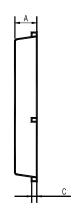


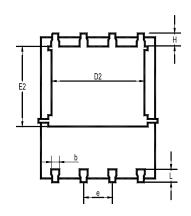


Package Outline Dimensions (Units: mm)

DFN5060

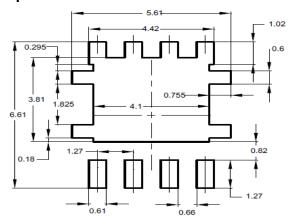






UNIT	Α	b	С	D	D1	D2	E	E1	E2	е	L	L1	Н
100 100	1.12	0.51	0.34	5.26	5.1	4. 5	6.25	6	3.66	1.37	0.71	0.2	0.71
mm	0.9	0.33	0.11	4.7	4.7	3.56	5.75	5.6	3.18	1.17	0.35	0.06	0.35

Recommended Soldering Footprint



Packing information

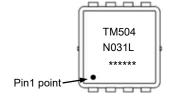
Package	Tape Width	Pit	tch	Reel Size		Per Reel Packing Quantity
rackage	(mm)	mm	inch	mm	inch	Fel Reel Facking Quantity
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	3,000

Marking information

" TM504N031L " = Part No.

" ***** " = Date Code Marking

Font type: Arial





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