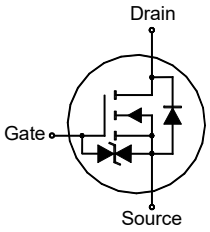
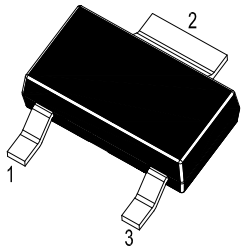
WPDQ90N1K5K-AH

N-Channel Enhancement Mode MOSFET





1.Gate 2.Drain 3.Source
SOT-223-2 Plastic Package

Features

- AEC-Q101 Qualified
- Halogen and Antimony Free(HAF), RoHS compliant
- ESD Protected
- Typical ESD Protection HBM Class 1C

Classification	Voltage Range(V)
0A	< 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

Key Parameters

Parameter	Value	Unit
BV_{DSS}	900	V
$R_{DS(ON)}$ Max	1.4 @ V_{GS} = 10 V	Ω
$V_{GS(th)}$ typ	3	V
Q_g typ	11 @ V_{GS} = 10 V	nC

Application

- Offline Power Supply

Absolute Maximum Ratings(at T_a = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	900	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	T_c = 25℃ T_c = 100℃	I_D	2 1.4	A
Peak Drain Current, Pulsed [1]		I_{DM}	7	A
Avalanche Current		I_{AS}	1.3	A
Single Pulse Avalanche Energy [2]		E_{AS}	76	mJ
Power Dissipation	T_c = 25℃	P_D	12.5	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	10	℃/W
Thermal Resistance from Junction to Ambient [3]	$R_{\theta JA}$	50	℃/W

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 150°C.

[2] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 86 mH, R_g = 25 Ω, I_D = 1.3 A, V_{GS} = 10 V.

[3] Device Surface Mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate, in a still air.

Dated: 26/03/2021 DF2A Rev: 01

Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 1 mA	BV_{DSS}	900	-	-	V
Drain-Source Leakage Current at V_{DS} = 900 V	I_{DSS}	-	-	1	µA
Gate Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 1	µA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 150 µA	$V_{GS(th)}$	2	-	4	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 0.9 A	$R_{DS(on)}$	-	1.1	1.4	Ω
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 0.9 A	g_{fs}	-	2	-	S
Gate Resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	R_g	-	4.9	-	Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = 450 V, f = 1 MHz	C_{iss}	-	457	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 450 V, f = 1 MHz	C_{oss}	-	11.4	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 450 V, f = 1 MHz	C_{rss}	-	2	-	pF
Gate charge total at V_{DS} = 450 V, I_D = 2 A, V_{GS} = 10 V	Q_g	-	11	-	nC
Gate to Source Charge at V_{DS} = 450 V, I_D = 2 A, V_{GS} = 10 V	Q_{gs}	-	3	-	nC
Gate to Drain Charge at V_{DS} = 450 V, I_D = 2 A, V_{GS} = 10 V	Q_{gd}	-	3.6	-	nC
Turn-On Delay Time at V_{DS} = 500 V, V_{GS} = 10 V, I_D = 2 A, R_g = 24 Ω	$t_{d(on)}$	-	26	-	ns
Turn-On Rise Time at V_{DS} = 500 V, V_{GS} = 10 V, I_D = 2 A, R_g = 24 Ω	t_r	-	21	-	ns
Turn-Off Delay Time at V_{DS} = 500 V, V_{GS} = 10 V, I_D = 2 A, R_g = 24 Ω	$t_{d(off)}$	-	25	-	ns
Turn-Off Fall Time at V_{DS} = 500 V, V_{GS} = 10 V, I_D = 2 A, R_g = 24 Ω	t_f	-	98	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 2 A, V_{GS} = 0 V	V_{SD}	-	-	1.3	V
Body-Diode Continuous Current	I_S	-	-	2	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	7	A
Body Diode Reverse Recovery Time at I_S = 2 A, di/dt = 100 A / µs	t_{rr}	-	222	-	ns
Body Diode Reverse Recovery Charge at I_S = 2 A, di/dt = 100 A / µs	Q_{rr}	-	1.6	-	µC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

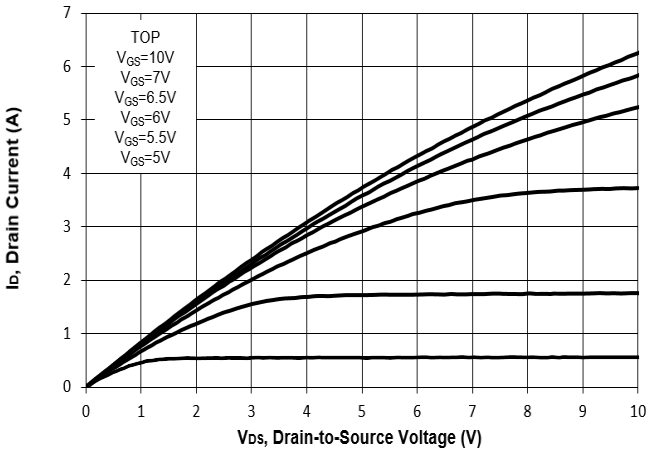


Fig. 2 Typical Transfer Characteristic

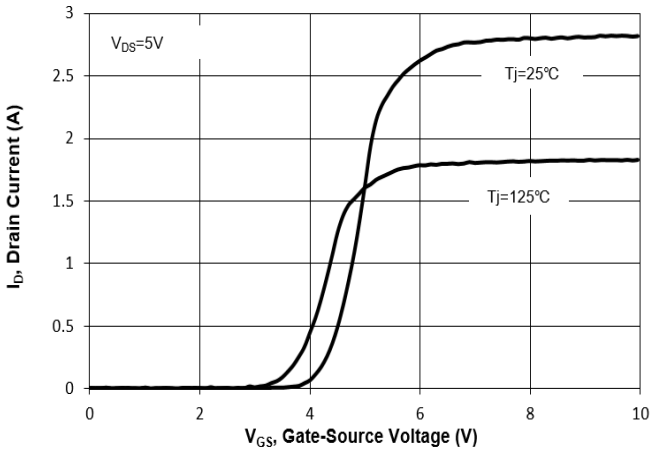


Fig. 3 On-Resistance vs. Drain Current

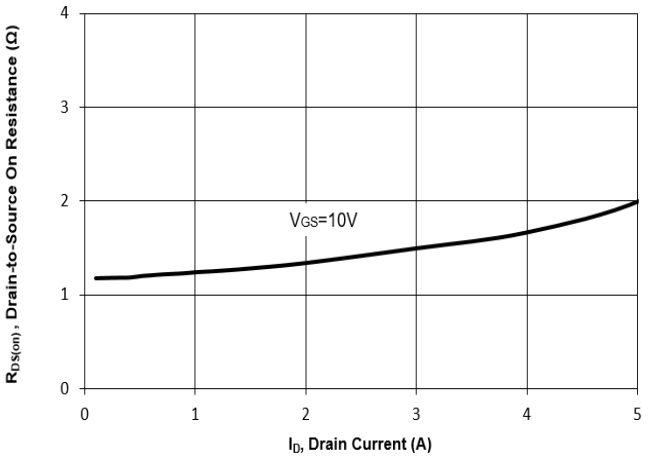


Fig. 4 On-Resistance vs. Gate Voltage

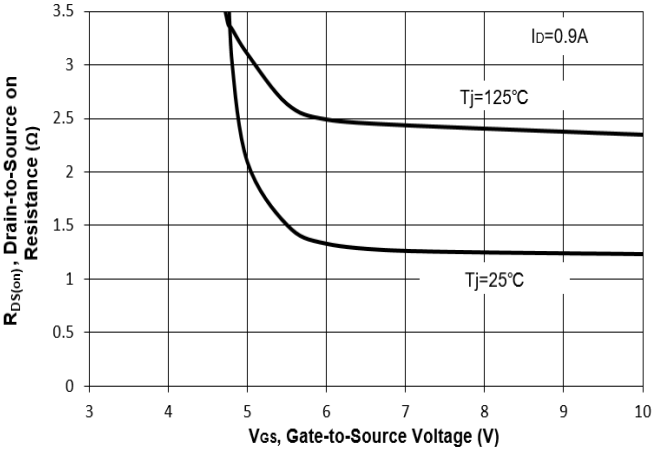


Fig. 5 On-Resistance vs.T_j

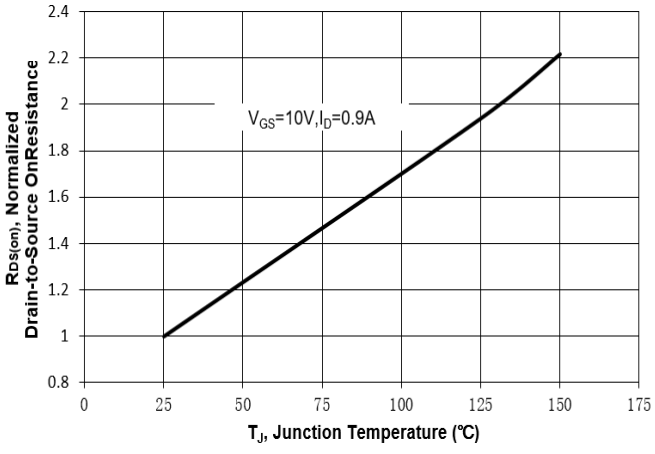
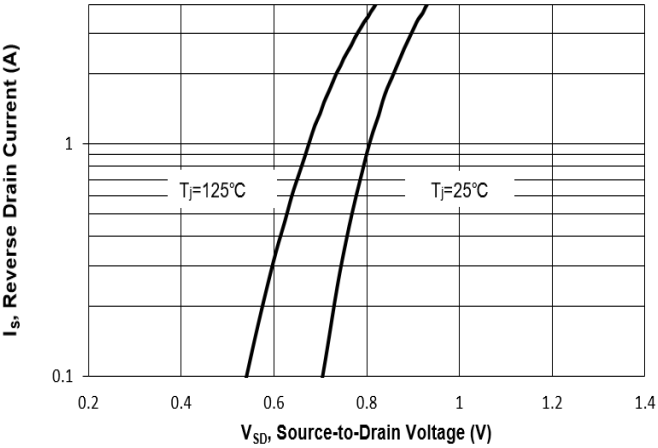


Fig. 6 Typical Body-Diode Forward Characteristic



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

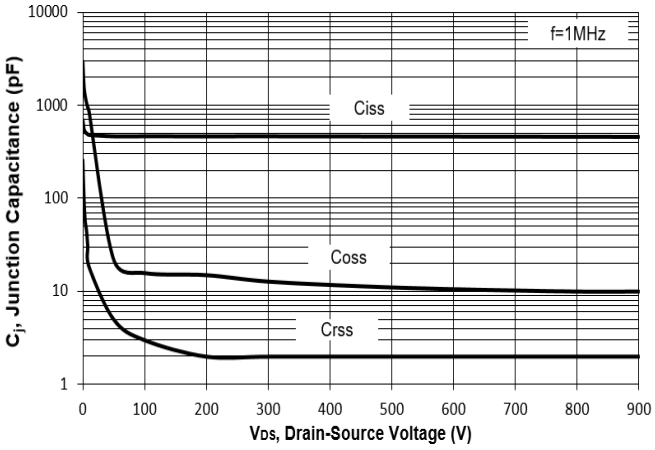


Fig. 8 Drain-Source Leakage Current vs. T_j

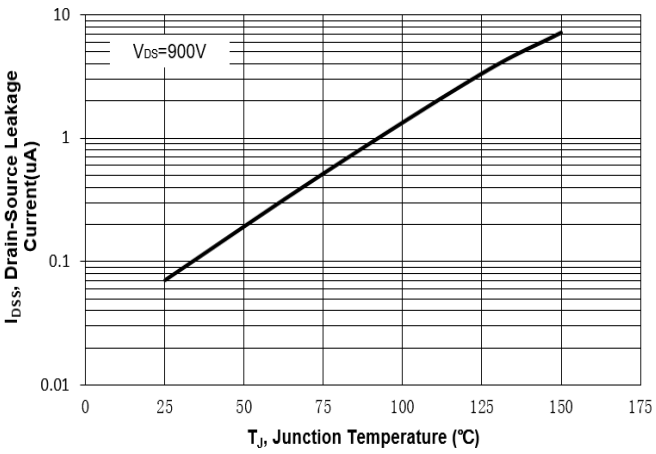


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

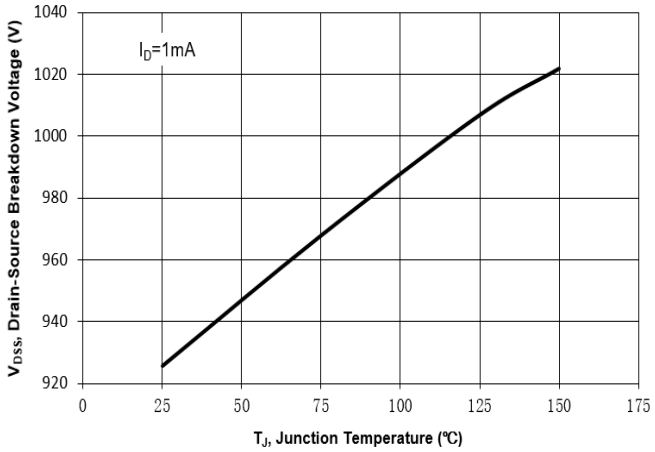


Fig. 10 Gate Threshold Variation vs. T_j

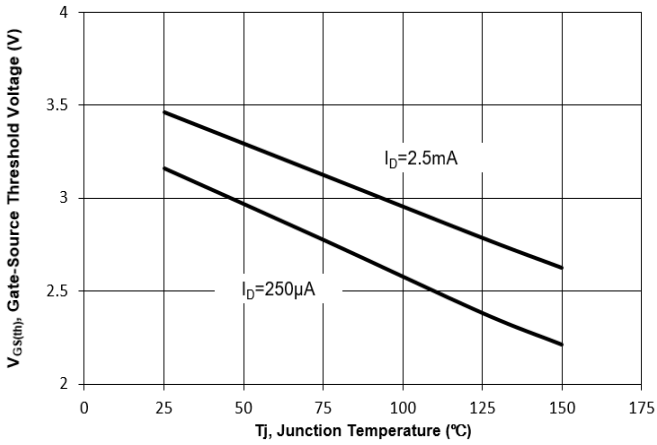


Fig. 11 Gate Charge

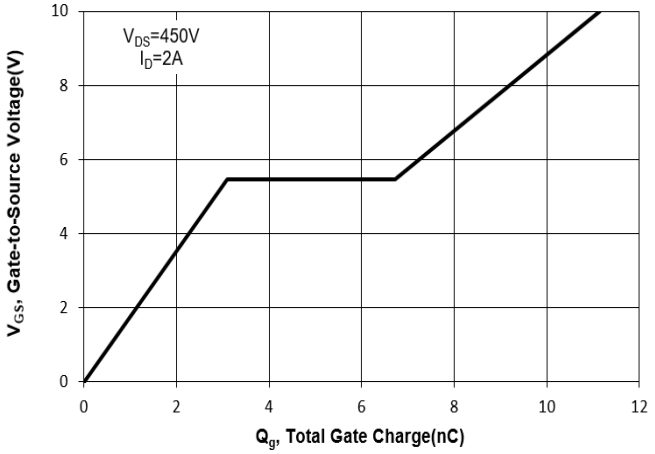
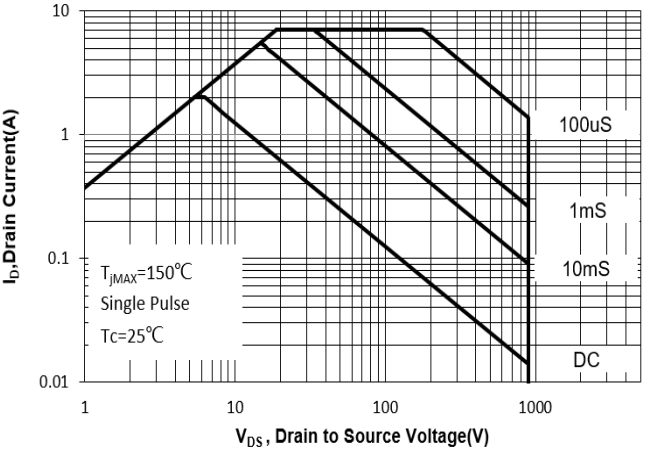


Fig. 12 Safe Operation Area



Electrical Characteristics Curves

Fig.13 Normalized Maximum Transient Thermal Impedance($z_{\theta JC}$)

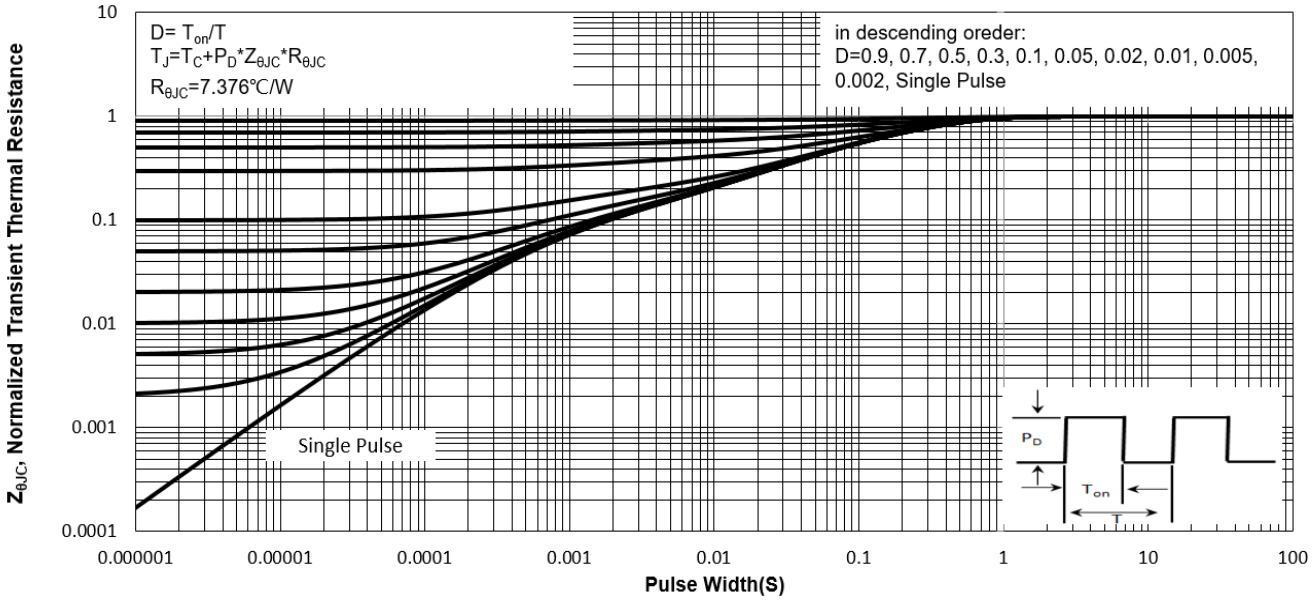
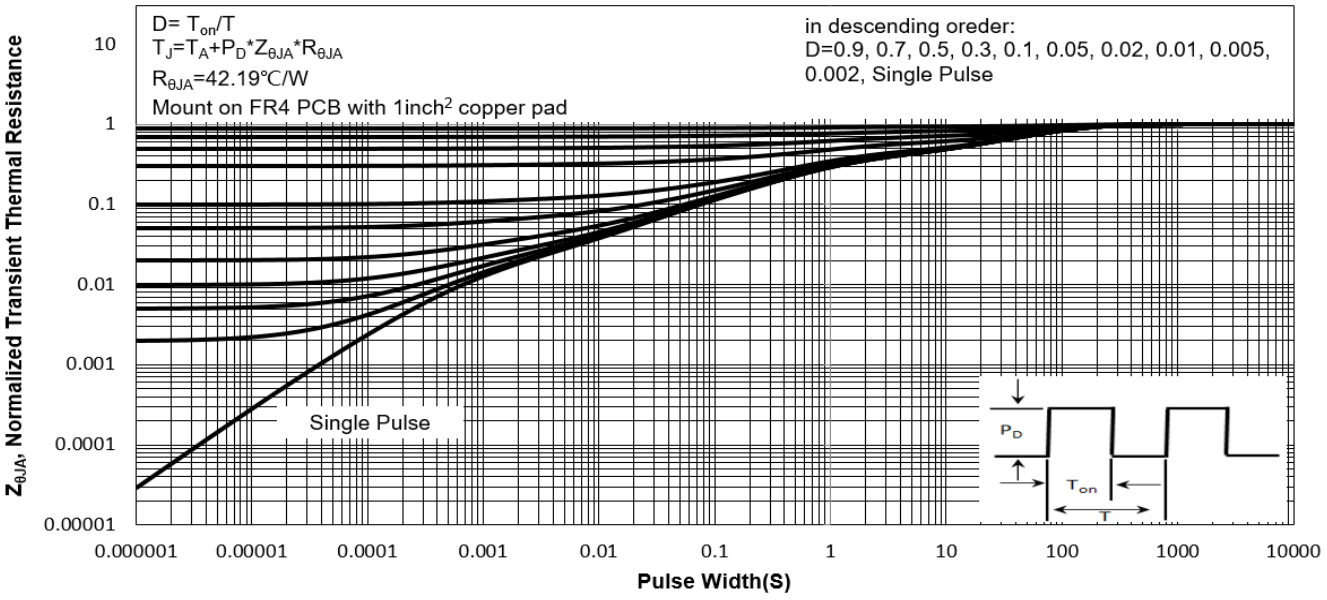


Fig.14 Normalized Maximum Transient Thermal Impedance($z_{\theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

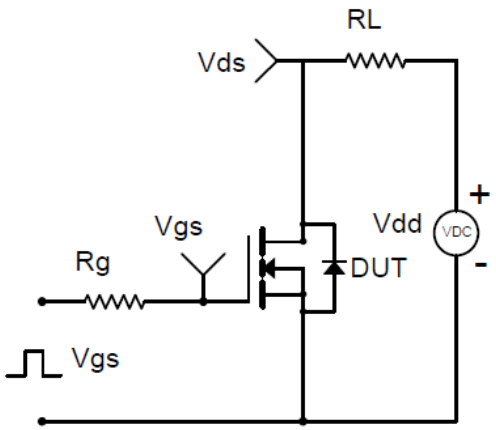


Fig.1-2 Switching Waveform

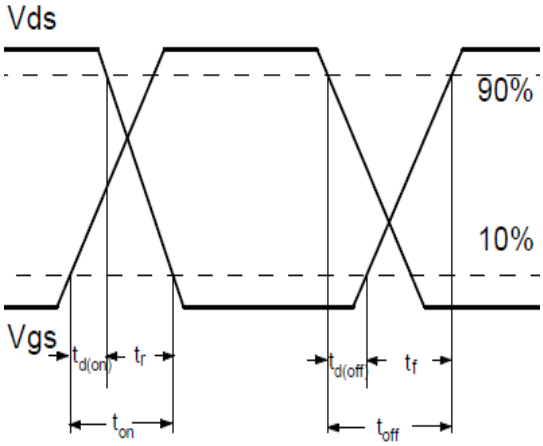


Fig.2-1 Gate charge test circuit

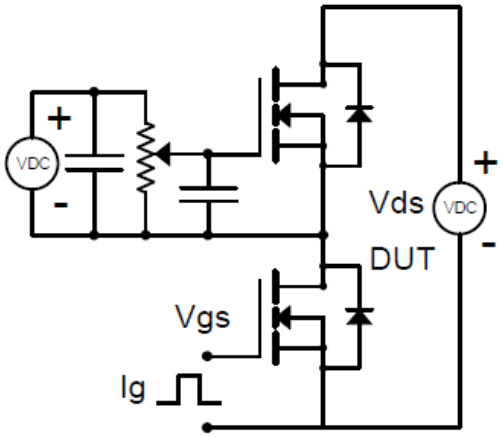


Fig.2-2 Gate charge waveform

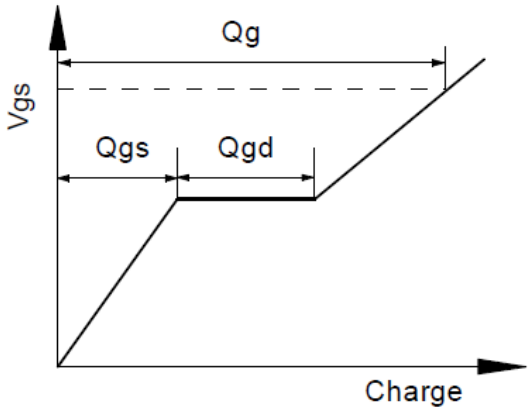


Fig.3-1 Avalanche test circuit

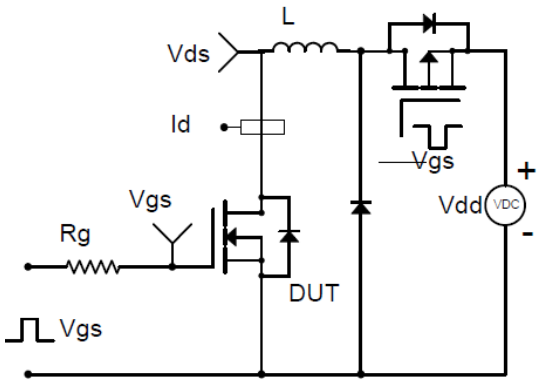
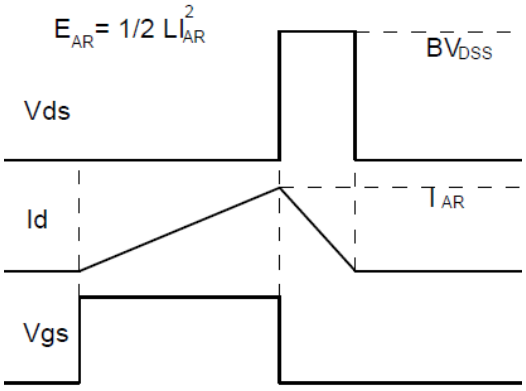
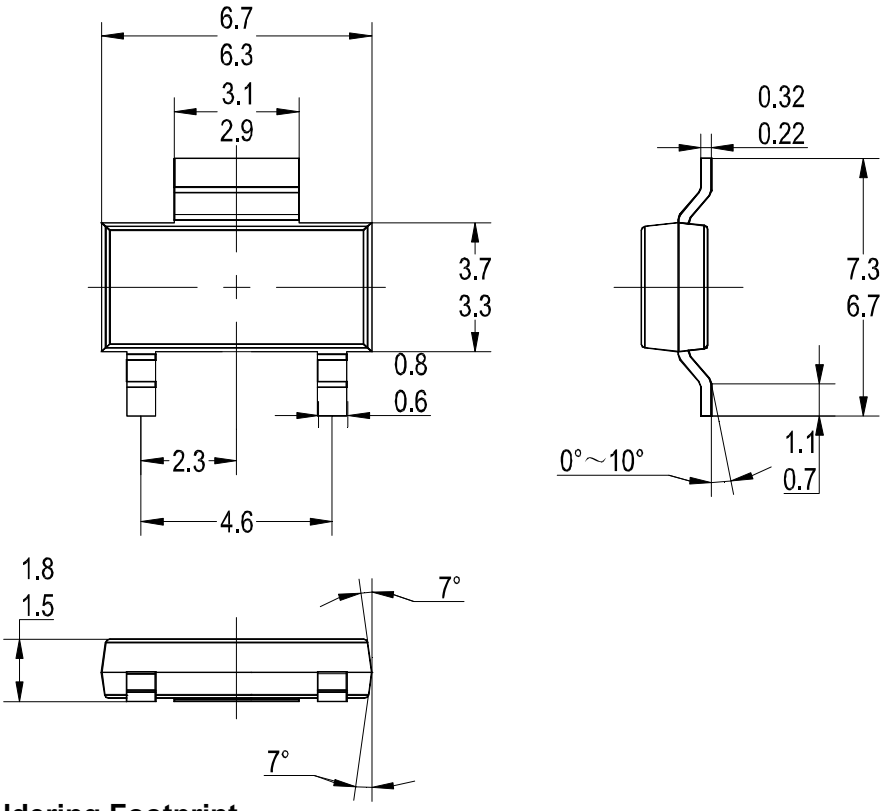


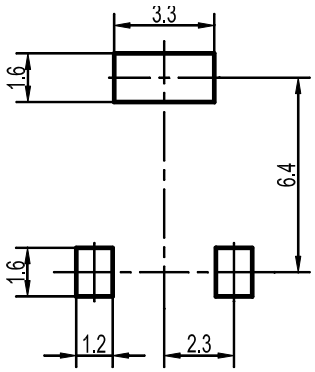
Fig.3-2 Avalanche waveform



PACKAGE OUTLINE (Dimensions in mm) SOT-223-2



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-223-2	12	4 ± 0.1	0.157 ± 0.004	330	13	3,000

Marking information

" PDQ90N1K5K " = Part No.

" ****** " = Date Code Marking

Font type: Arial

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