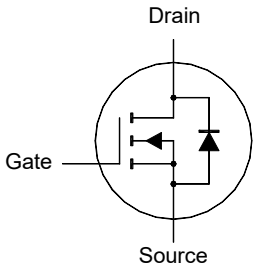
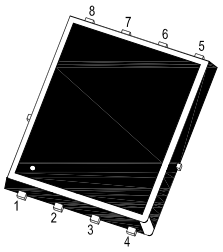
WDM504N031L-AH

N-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 Qualified
- Low $R_{DS(on)}$ to minimize conduction losses
- Low capacitance to minimize driver losses
- Halogen and Antimony Free(HAF), RoHS compliant





1. Source 2. Source 3. Source 4. Gate
5. Drain 6. Drain 7. Drain 8. Drain
DFN5060 Plastic Package

Application

- Synchronous buck converter

Key Parameters

Parameter	Value	Unit
BV_{DSS}	40	V
$R_{DS(ON)}$ Max	3.3 @ V_{GS} = 10 V	mΩ
	4.9 @ V_{GS} = 4.5 V	mΩ
$V_{GS(th)}$ typ	1.5	V
Q_g typ	45 @ V_{GS} = 10 V	nC

Absolute Maximum Ratings (at T_a = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T_c = 25℃ T_c = 100℃	I_D	75 47	A
Peak Drain Current [1]		I_{DM}	420	A
Avalanche Current		I_{AS}	40	A
Single Pulse Avalanche Energy [2]		E_{AS}	80	mJ
Power Dissipation	T_c = 25℃ T_c = 100℃	P_D	27.8 11	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	℃

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal Resistance from Junction to Case		$R_{\theta JC}$	4.5	℃/W
Thermal Resistance from Junction to Ambient [3]	Steady State	$R_{\theta JA}$	45	℃/W

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 150°C.

[2] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 0.1 mH, R_g = 25 Ω, I_D = 40 A, V_{GS} = 10 V.

[3] Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Dated: 23/10/2020 Rev: 01

Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 µA	BV_{DSS}	40	-	-	V
Drain-Source Leakage Current at V_{DS} = 40 V	I_{DSS}	-	-	1	µA
Gate Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	1.2	-	2.2	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 40 A at V_{GS} = 4.5 V, I_D = 40 A	$R_{DS(on)}$	- -	2.8 -	3.3 4.9	mΩ
DYNAMIC PARAMETERS					
Gate resistance at V_{DS} = 0 V, f = 1 MHz	R_g	-	2.2	-	Ω
Forward Transconductance at V_{DS} = 5 V, I_D = 40 A	g_{fs}	-	25	-	S
Input Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2225	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	956	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	52	-	pF
Gate charge total at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 10 V at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V	Q_g	- -	45 23	- -	nC
Gate to Source Charge at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V	Q_{gs}	-	8	-	nC
Gate to Drain Charge at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V	Q_{gd}	-	13	-	nC
Turn-On Delay Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	$t_{d(on)}$	-	29	-	nS
Turn-On Rise Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	t_r	-	107	-	nS
Turn-Off Delay Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	$t_{d(off)}$	-	22	-	nS
Turn-Off Fall Time at V_{DS} = 20 V, I_D = 40 A, V_{GS} = 4.5 V, R_g = 4.7 Ω	t_f	-	37	-	nS
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 40 A, V_{GS} = 0 V	V_{SD}	-	-	1.2	V
Body-Diode Continuous Current	I_S	-	-	75	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	420	A
Body Diode Reverse Recovery Time at I_S = 40 A, di/dt = 100 A / µs	t_{rr}	-	30	-	nS
Body Diode Reverse Recovery Charge at I_S = 40 A, di/dt = 100 A / µs	Q_{rr}	-	17	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

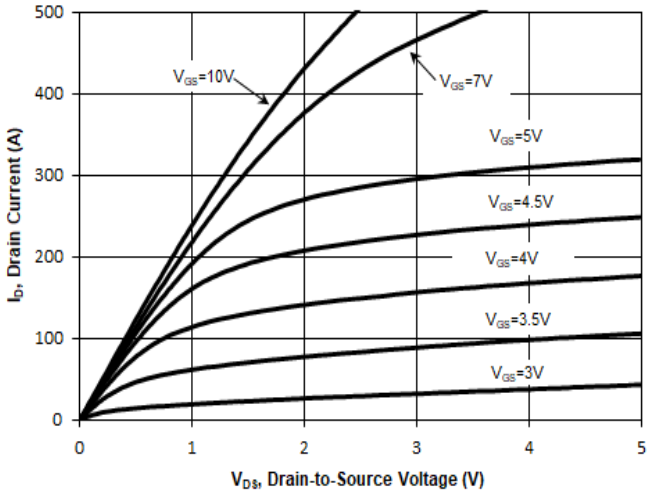


Fig. 2 Typical Transfer Characteristic

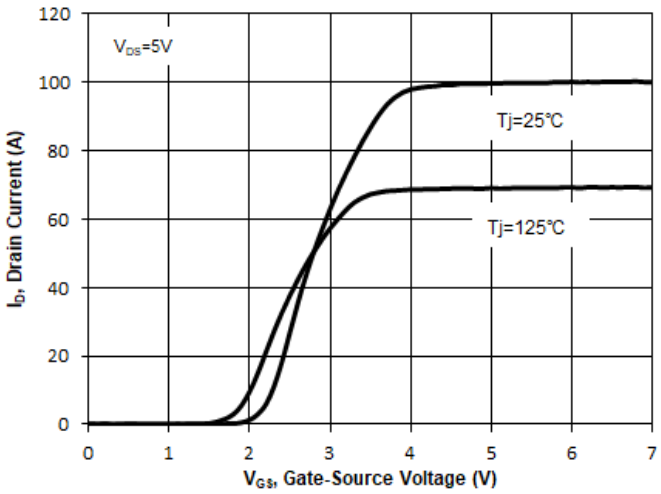


Fig. 3 on-Resistance vs. Drain Current

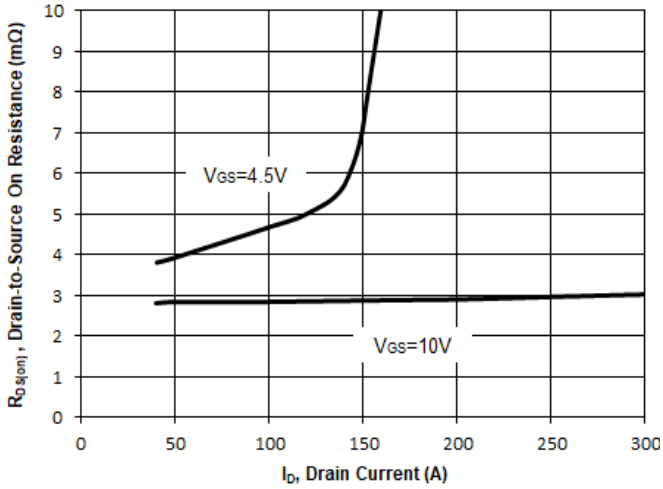


Fig. 4 on-Resistance vs. Gate Voltage

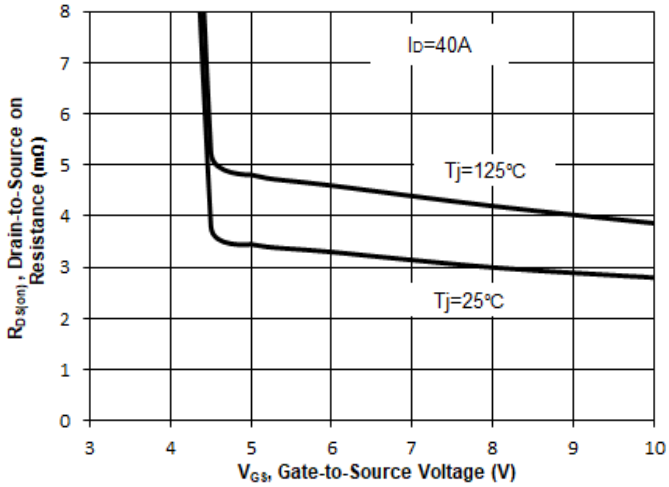


Fig. 5 on-Resistance vs.T_j

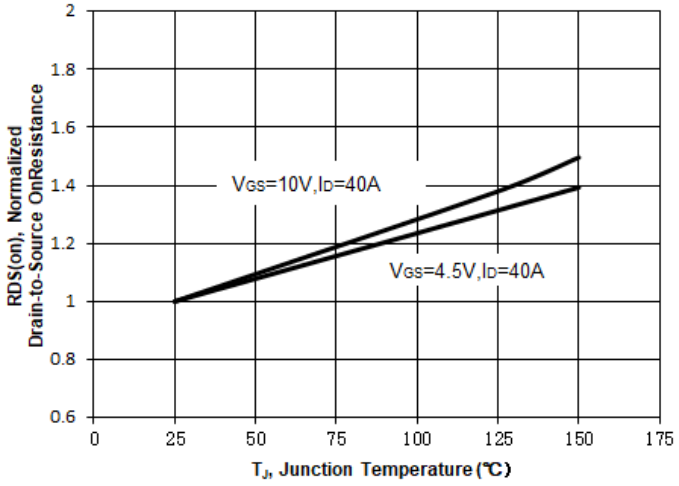
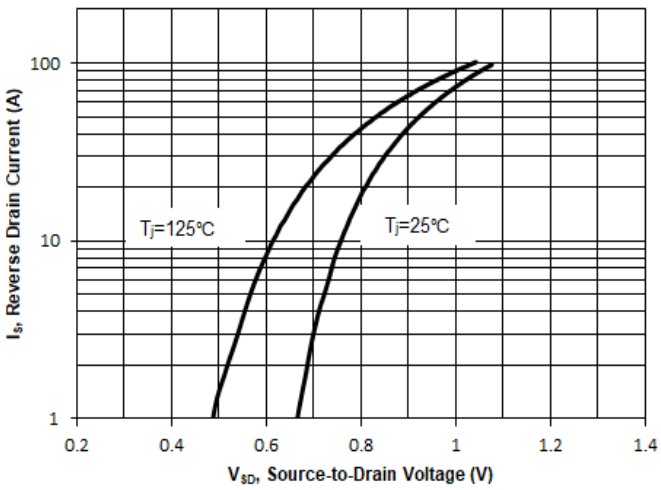


Fig. 6 Typical Forward Characteristic



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

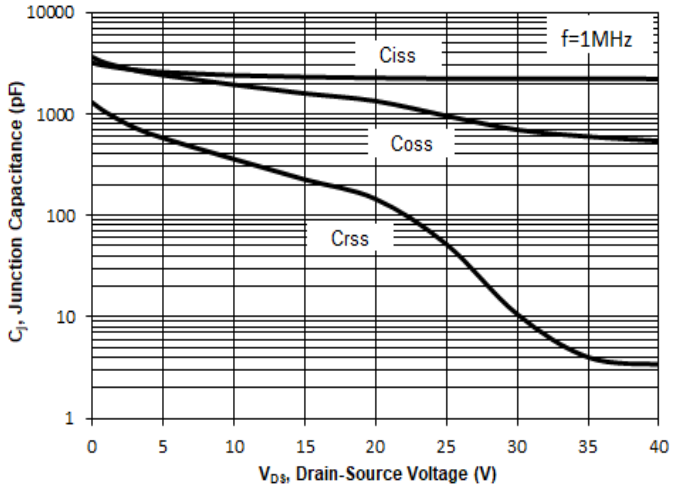


Fig. 8 Drain-Source Leakage Current vs. T_j

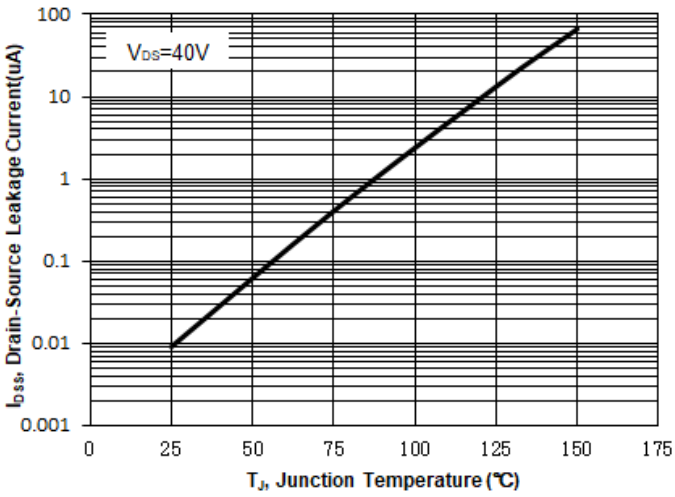


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

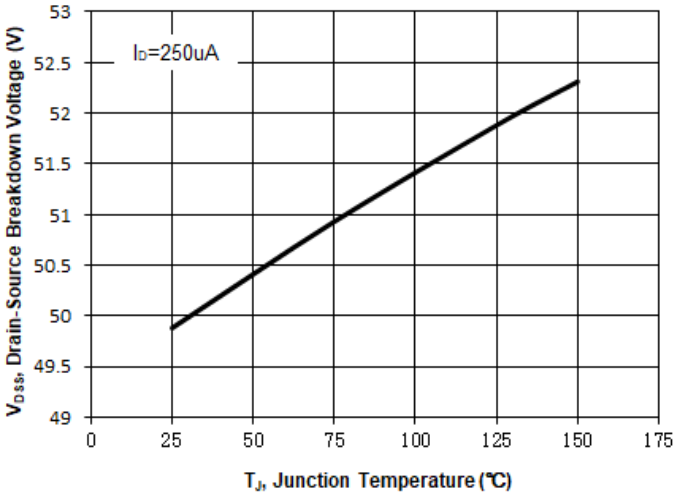


Fig. 10 Gate Threshold Variation vs. T_j

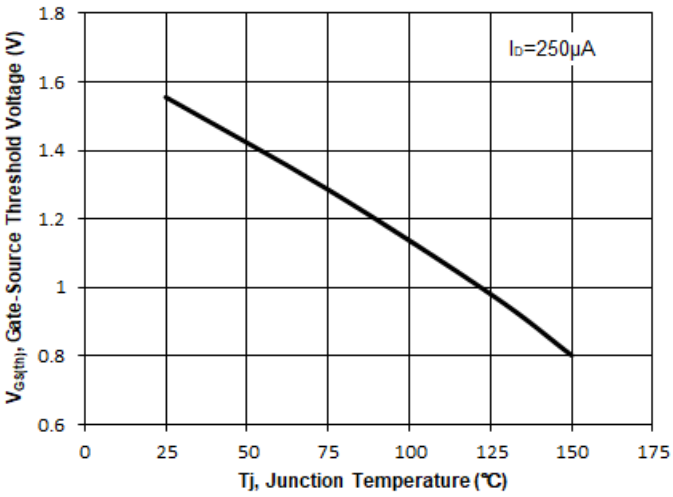


Fig. 11 Gate Charge

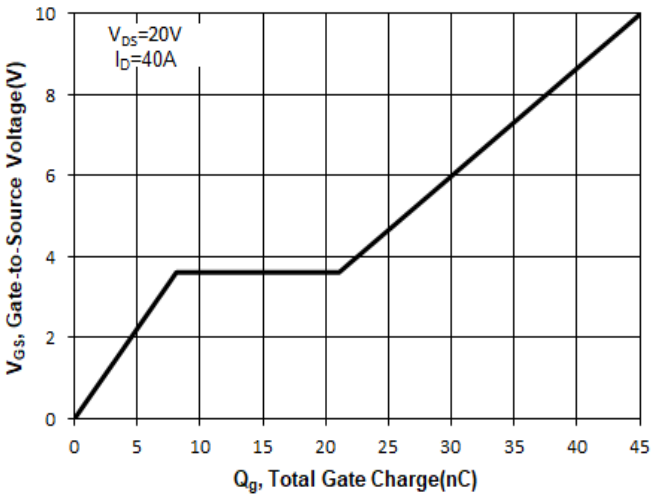
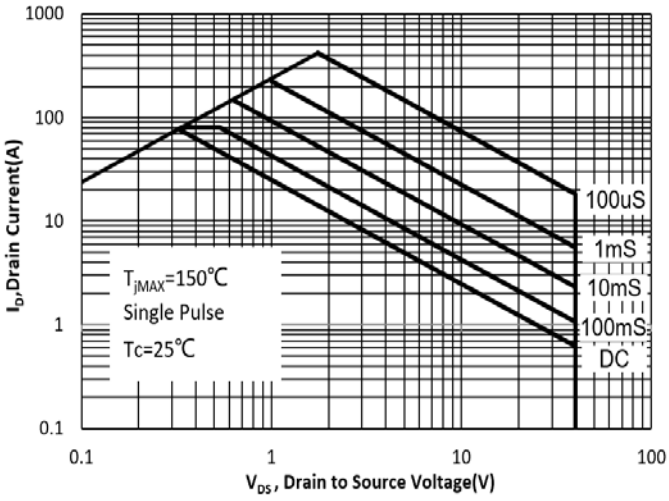


Fig. 12 Safe Operation Area



Electrical Characteristics Curves

Fig.13 Normalized Maximum Transient Thermal Impedance($z_{\Theta JA}$)

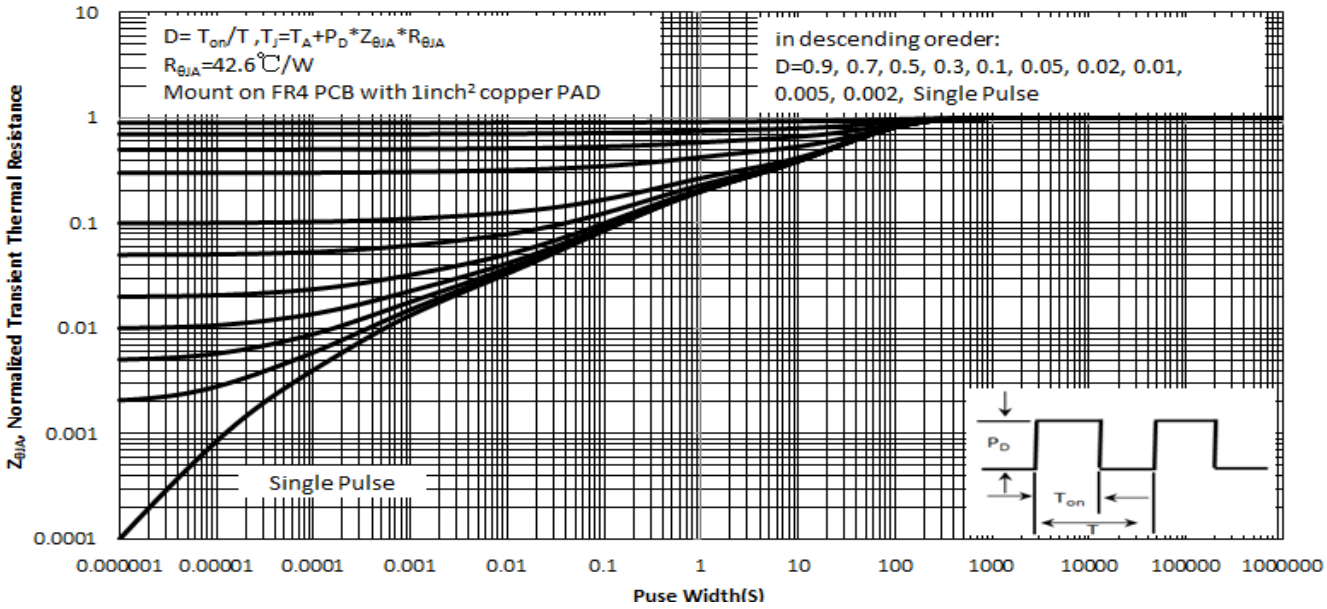
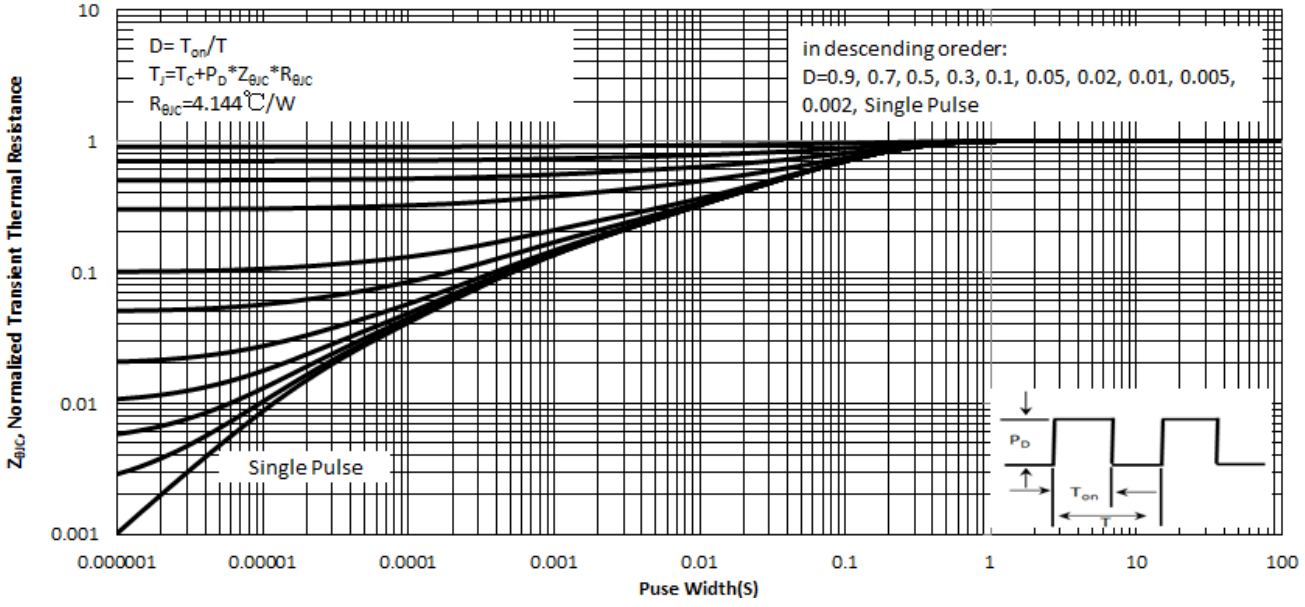


Fig.14 Normalized Maximum Transient Thermal Impedance($z_{\Theta JC}$)



Test Circuits

Fig.1-1 Switching times test circuit

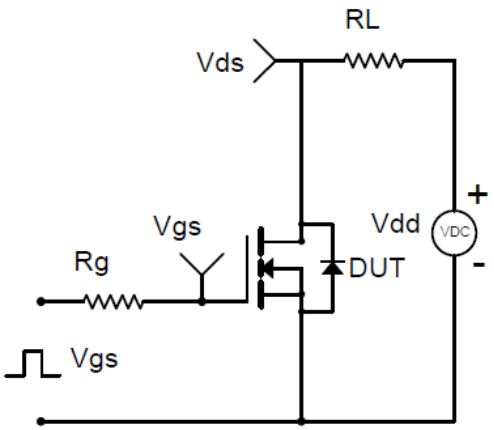


Fig.1-2 Switching Waveform

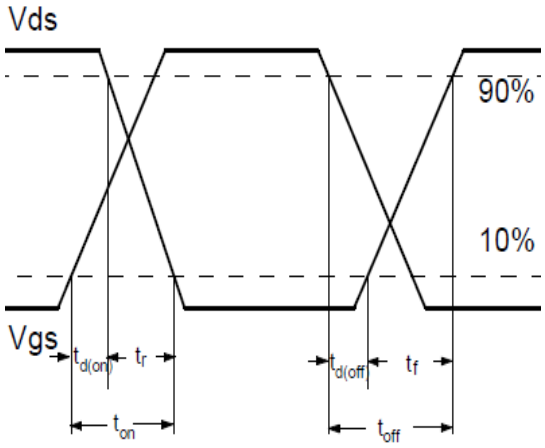


Fig.2-1 Gate charge test circuit

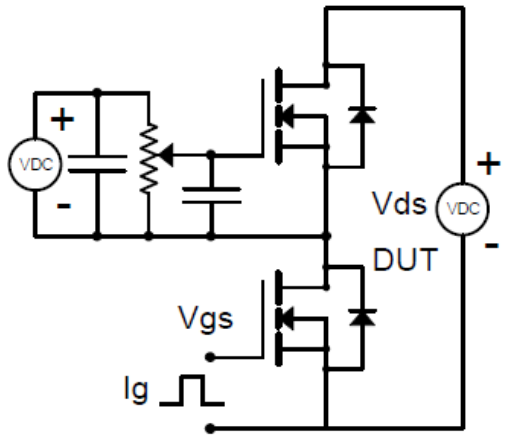


Fig.2-2 Gate charge waveform

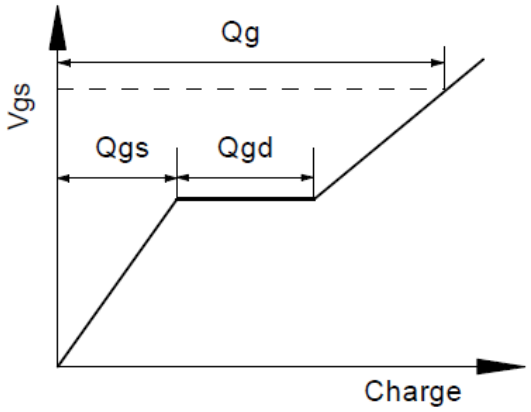


Fig.3-1 Avalanche test circuit

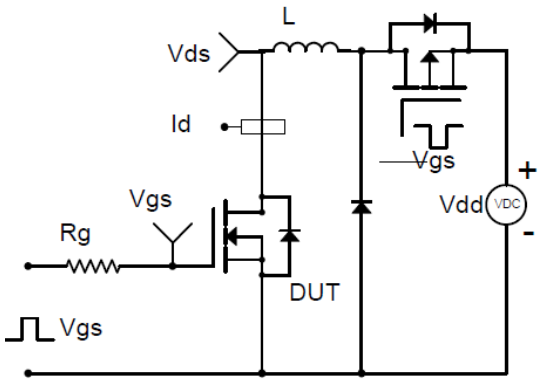
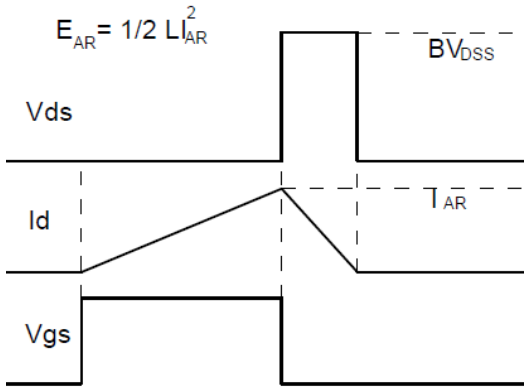
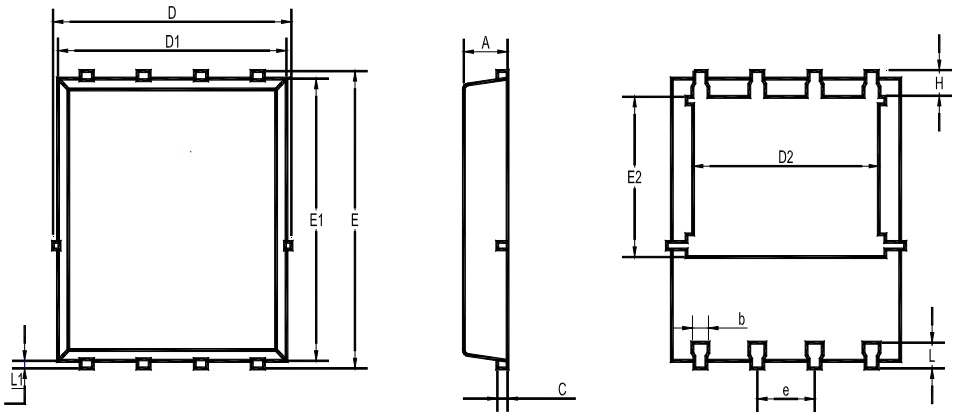


Fig.3-2 Avalanche waveform

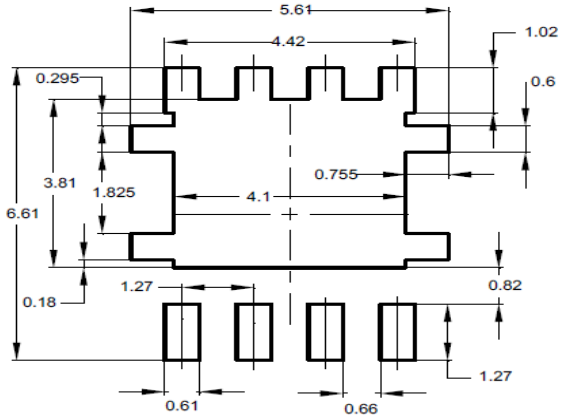


Package Outline Dimensions (Units: mm) DFN5060



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12 0.9	0.51 0.33	0.34 0.11	5.26 4.7	5.1 4.7	4. 5 3.56	6.25 5.75	6 5.6	3.66 3.18	1.37 1.17	0.71 0.35	0.2 0.06	0.71 0.35

Recommended Soldering Footprint

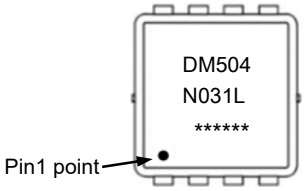


Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	3,000

Marking information

" DM504N031L " = Part No.
" ****** " = Date Code Marking
Font type: Arial



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