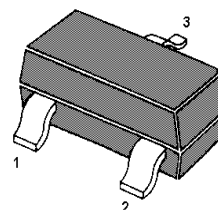
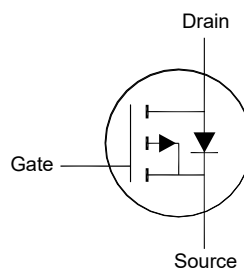


MMFTP3409-AH

P-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 is Available
- Halogen and Antimony Free(HAF),
RoHS complian



1. Gate 2. Source 3. Drain
TO-236 Plastic Package

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$ unless otherwise specified)

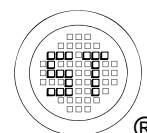
Parameter	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DS}$	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	$-I_D$	2.6	A
Peak Drain Current, Pulsed ¹⁾	$-I_{DM}$	20	A
Power Dissipation	P_D	1.4	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance - Junction to Ambient ²⁾ $t \leq 10 \text{ S}$ Steady State	$R_{\theta JA}$	90 125	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width $\leq 100 \mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})} = 150^\circ\text{C}$

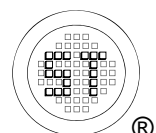
²⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.



MMFTP3409-AH

Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $-I_D = 250\ \mu\text{A}$	$-V_{(BR)DSS}$	30	-	-	V
Drain-Source On-State Current at $-V_{DS} = 24\ \text{V}$	$-I_{DSS}$	-	-	1	μA
Gate-Source Leakage Current at $V_{GS} = \pm 20\ \text{V}$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at $-V_{DS} = V_{GS}$, $-I_D = 250\ \mu\text{A}$	$-V_{GS(th)}$	1	-	2	V
Drain-Source On-State Resistance at $-V_{GS} = 10\ \text{V}$, $-I_D = 2.6\ \text{A}$ at $-V_{GS} = 4.5\ \text{V}$, $-I_D = 2\ \text{A}$	$R_{DS(ON)}$	- -	- -	90 160	m Ω
DYNAMIC PARAMETERS					
Gate resistance at $-V_{DS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	R_g	-	21	-	Ω
Forward Transconductance at $-V_{DS} = 5\ \text{V}$, $-I_D = 2.5\ \text{A}$	g_{fs}	3	-	-	S
Input Capacitance at $-V_{GS} = 0\ \text{V}$, $-V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{iss}	-	441	-	pF
Output Capacitance at $-V_{GS} = 0\ \text{V}$, $-V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{oss}	-	41	-	pF
Reverse Transfer Capacitance at $-V_{GS} = 0\ \text{V}$, $-V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{rss}	-	35	-	pF
Total Gate Charge at $-V_{GS} = 10\ \text{V}$, $-V_{DS} = 15\ \text{V}$, $-I_D = 2.6\ \text{A}$ at $-V_{GS} = 4.5\ \text{V}$, $-V_{DS} = 15\ \text{V}$, $-I_D = 2.6\ \text{A}$	Q_g	- -	9 4.5	- -	nC
Gate-Source Charge at $-V_{GS} = 10\ \text{V}$, $-V_{DS} = 15\ \text{V}$, $-I_D = 2.6\ \text{A}$	Q_{gs}	-	3	-	nC
Gate-Drain Charge at $-V_{GS} = 10\ \text{V}$, $-V_{DS} = 15\ \text{V}$, $-I_D = 2.6\ \text{A}$	Q_{gd}	-	1.2	-	nC
Turn-On Delay Time at $-V_{DS} = 15\ \text{V}$, $-V_{GS} = 10\ \text{V}$, $R_G = 3.3\ \Omega$, $R_L = 5.8\ \Omega$	$t_{d(on)}$	-	7.5	-	ns
Turn-On Rise Time at $-V_{DS} = 15\ \text{V}$, $-V_{GS} = 10\ \text{V}$, $R_G = 3.3\ \Omega$, $R_L = 5.8\ \Omega$	t_r	-	3.2	-	ns
Turn-Off Delay Time at $-V_{DS} = 15\ \text{V}$, $-V_{GS} = 10\ \text{V}$, $R_G = 3.3\ \Omega$, $R_L = 5.8\ \Omega$	$t_{d(off)}$	-	17	-	ns
Turn-Off Fall Time at $-V_{DS} = 15\ \text{V}$, $-V_{GS} = 10\ \text{V}$, $R_G = 3.3\ \Omega$, $R_L = 5.8\ \Omega$	t_f	-	6.8	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $-I_F = 1\ \text{A}$, $-V_{GS} = 0\ \text{V}$	$-V_{SD}$	-	-	1	V
Body Diode Reverse Recovery Time at $-I_F = 2.6\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	t_{rr}	-	7	-	ns
Body Diode Reverse Recovery Charge at $-I_F = 2.6\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	Q_{rr}	-	3	-	nC



Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

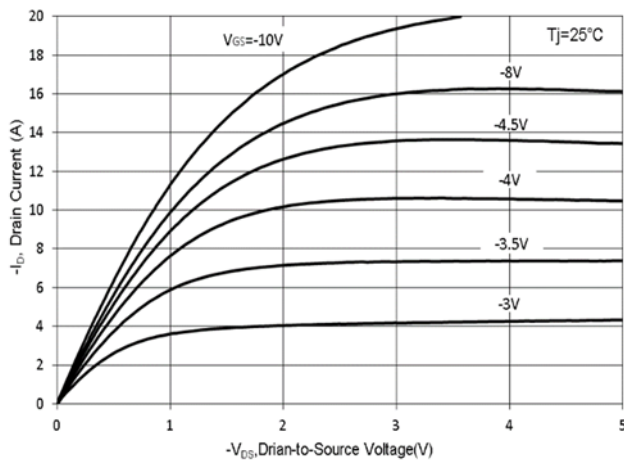


Fig. 2 Drain Current Vs Gate Voltage

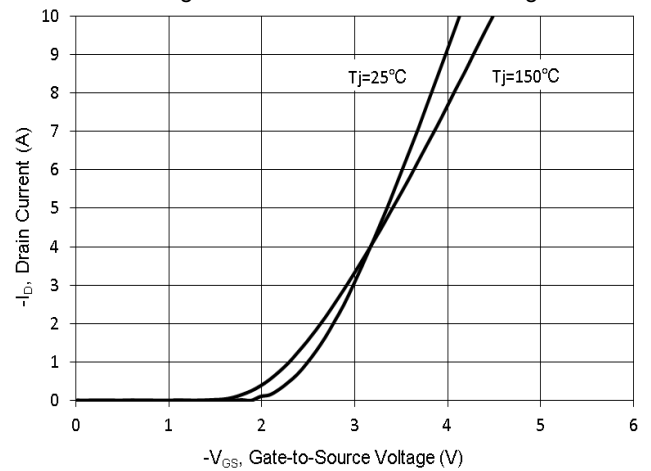


Fig. 3 On-Resistance Vs Gate Voltage

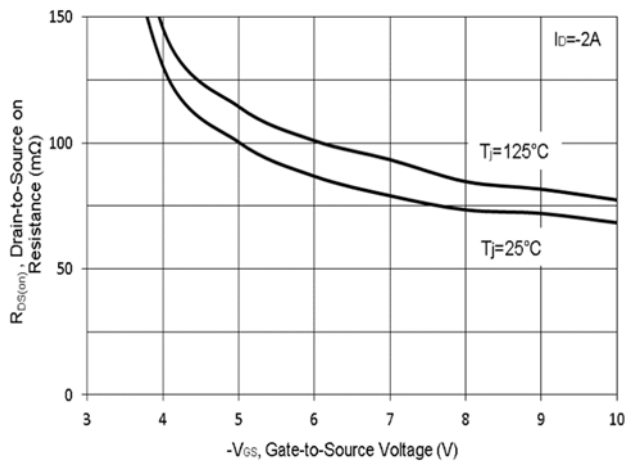


Fig. 4 On-Resistance Vs Tj

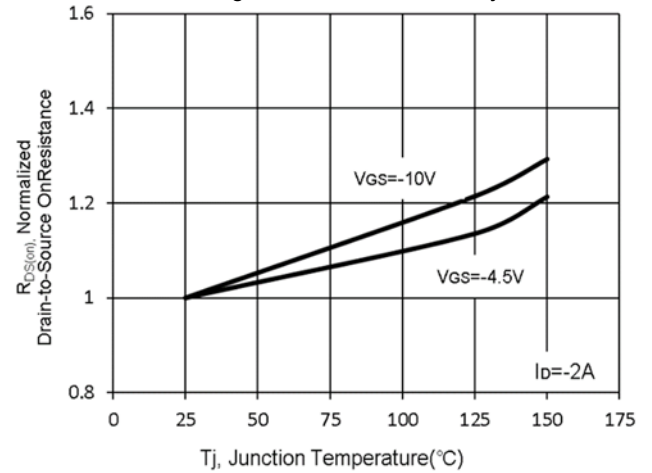


Fig. 5 On-Resistance Vs Drain Current

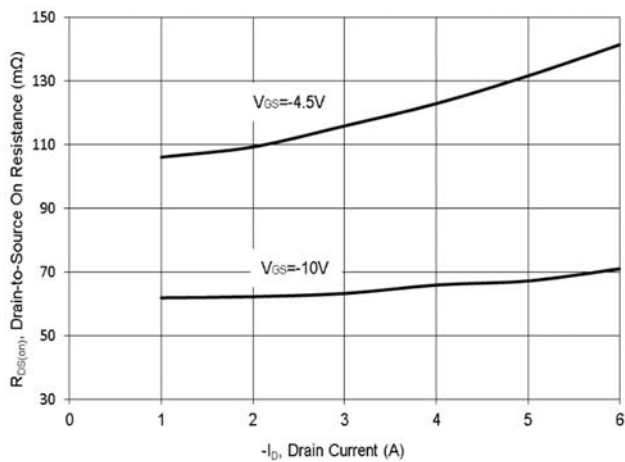
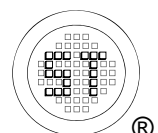
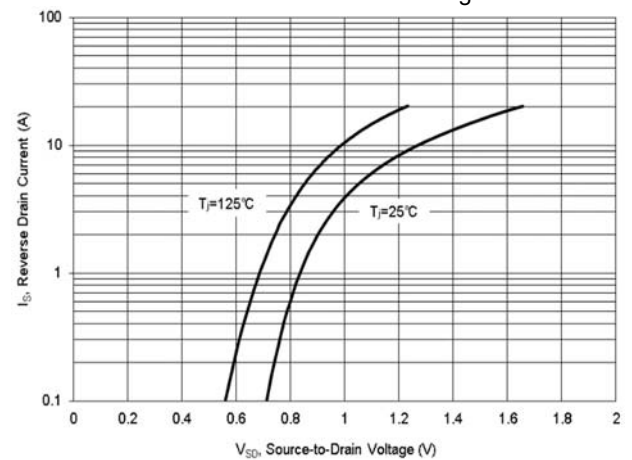


Fig. 6 Reverse Drain Current Vs Source-to-Drain Voltage



Electrical Characteristics Curves

Fig. 7 Drain-Source Leakage Current Vs Tj

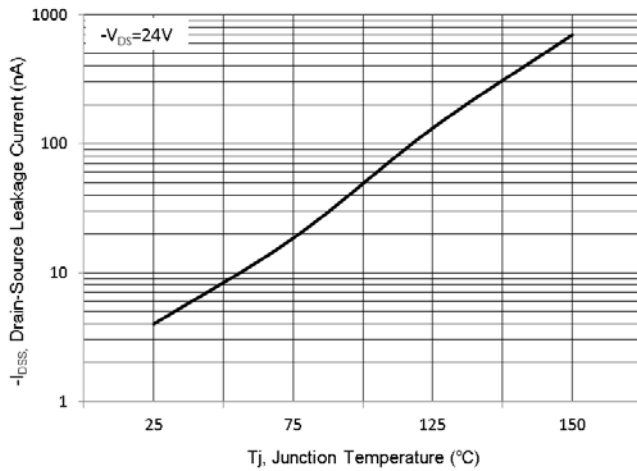


Fig. 8 Gate Charge

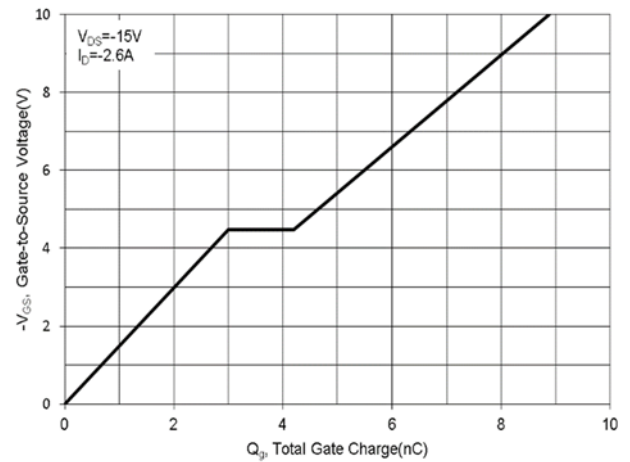


Fig. 9 Gate Threshold Variation Vs Tj

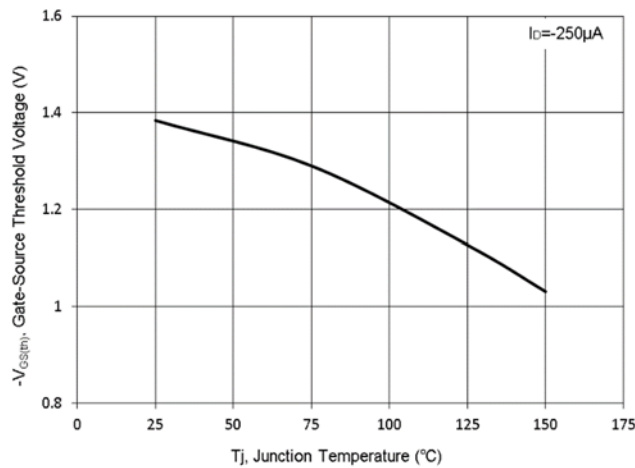


Fig. 10 $V_{(BR)DSS}$ Vs Junction Temperature

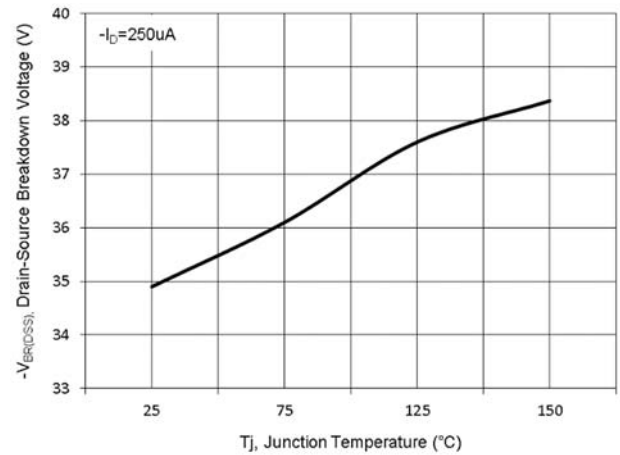


Fig. 11 Typical Junction Capacitance

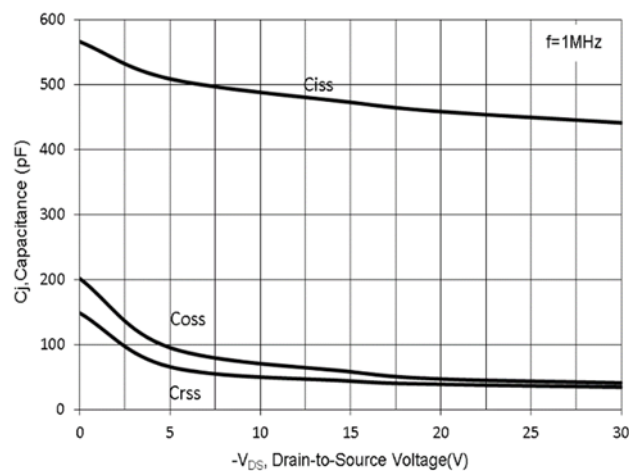
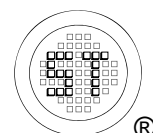
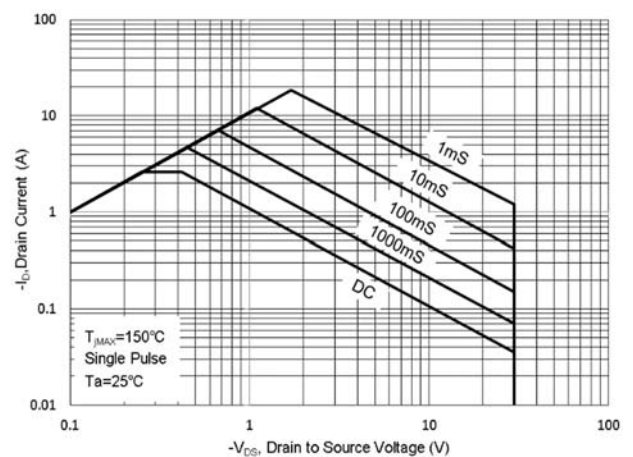


Fig. 12 SOA, Safe Operation Area



Test Circuits

Fig.1-1 Switching times test circuit

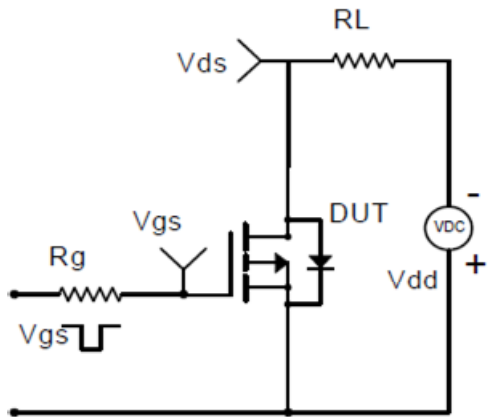


Fig.1-2 Switching Waveform

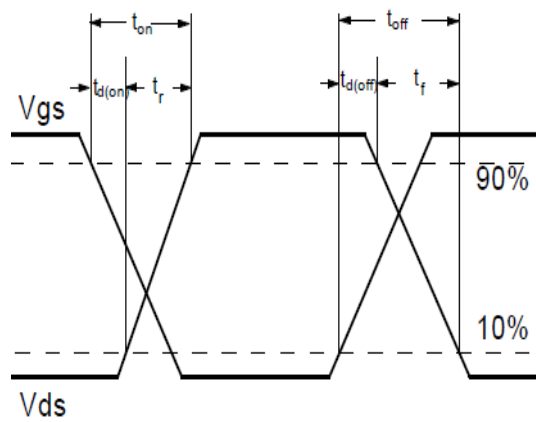


Fig.2-1 Gate charge test circuit

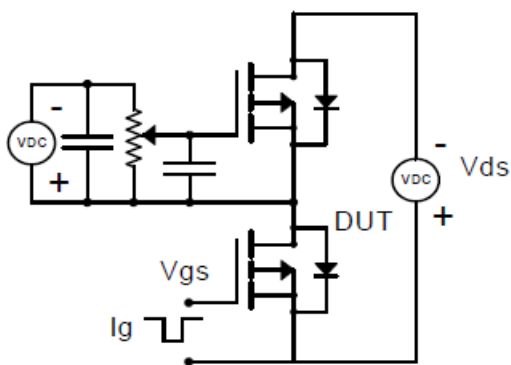
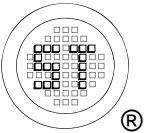
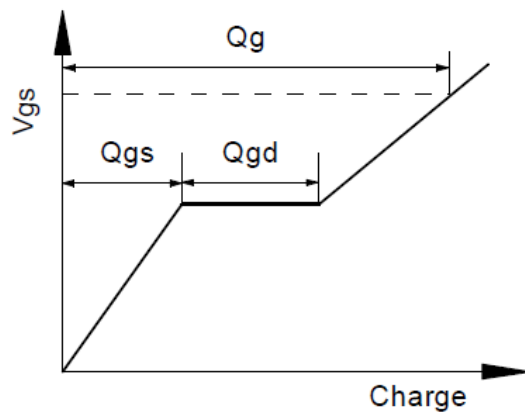
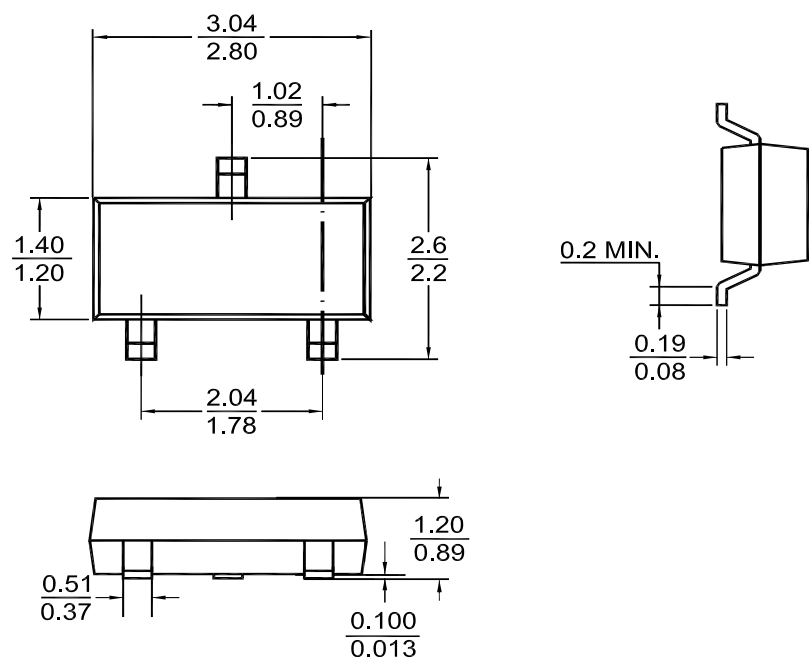


Fig.2-2 Gate charge waveform

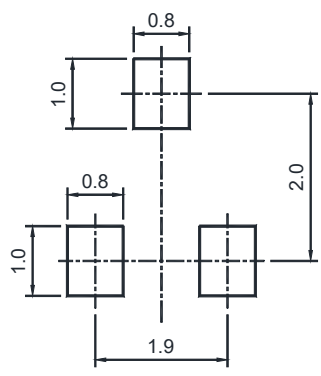


Package Outline (Dimensions in mm)

TO-236



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
TO-236	8	4 ± 0.1	0.157 ± 0.004	178	7	3,000

Marking information

" VK " = Part No.
" • " = HAF (Halogen and Antimony Free)
" YM " = Date Code Marking
" Y " = Year
" M " = Month
Font type: Arial

