MMFTP2301B

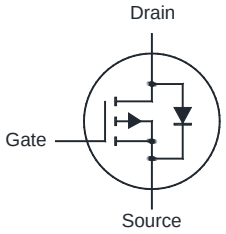
P-Channel Enhancement Mode MOSFET

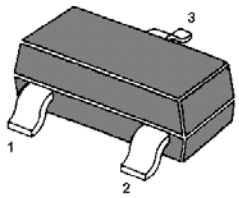
Features

• Advanced trench cell design

Applications

• LCD TV appliances
• High power inverter system





1. Gate 2. Source 3. Drain
TO-236 Plastic Package

Absolute Maximum Ratings at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DS}$	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Drain Current	$-I_D$	2.8	A
Peak Drain Current [1]	$-I_{DM}$	8	A
Power Dissipation T_a = 25℃ T_a = 75℃	P_{tot}	0.9 0.57	W
Thermal Resistance from Juntion to Ambient (PCB mounted) [2]	$R_{\theta JA}$	140	℃/W
Operating Junction and Storage Temperature Range	T_J,T_{stg}	- 55 to + 150	℃

[1] Repetitive rating, pulse width limited by junction temperature $T_{j(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial Tj = 25°C.

[2] Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Dated: 14/05/2020 Rev: 03

Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $-I_D$ = 250 µA	$-BV_{DSS}$	20	-	-	V
Drain-Source Leakage Current at $-V_{DS}$ = 20 V	$-I_{DSS}$	-	-	1	µA
Gate Leakage Current at V_{GS} = ± 8 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, $-I_D$ = 250 µA	$-V_{GS(th)}$	0.4	-	0.9	V
Drain-Source On-State Resistance at $-V_{GS}$ = 4.5 V, $-I_D$ = 2.8 A at $-V_{GS}$ = 2.5 V, $-I_D$ = 2 A	$R_{DS(on)}$	- -	- -	100 150	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at $-V_{DS}$ = 5 V, $-I_D$ = 4 A	g_{FS}	-	8	-	S
Gate Resistance at f = 1 MHz	R_g	-	7	-	Ω
Input Capacitance at V_{GS} = 0 V, $-V_{DS}$ = 10 V, f = 1 MHz	C_{iss}	-	354	-	pF
Output Capacitance at V_{GS} = 0 V, $-V_{DS}$ = 10 V, f = 1 MHz	C_{oss}	-	48	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, $-V_{DS}$ = 10 V, f = 1 MHz	C_{rss}	-	28	-	pF
Total Gate Charge at $-V_{DS}$ = 10 V, $-V_{GS}$ = 4.5 V, $-I_D$ = 1 A	Q_g	-	4.9	-	nC
Gate-Source Charge at $-V_{DS}$ = 10 V, $-V_{GS}$ = 4.5 V, $-I_D$ = 1 A	Q_{gs}	-	1.4	-	nC
Gate-Drain Charge at $-V_{DS}$ = 10 V, $-V_{GS}$ = 4.5 V, $-I_D$ = 1 A	Q_{gd}	-	1.3	-	nC
Turn-On Delay Time at $-V_{DS}$ = 10 V, $-V_{GS}$ = 4.5 V, $-I_D$ = 1 A, R_G = 10 Ω	$t_{d(on)}$	-	8.4	-	ns
Turn-On Rise Time at $-V_{DS}$ = 10 V, $-V_{GS}$ = 4.5 V, $-I_D$ = 1 A, R_G = 10 Ω	t_r	-	11.8	-	ns
Turn-Off Delay Time at $-V_{DS}$ = 10 V, $-V_{GS}$ = 4.5 V, $-I_D$ = 1 A, R_G = 10 Ω	$t_{d(off)}$	-	32.4	-	ns
Turn-Off Fall Time at $-V_{DS}$ = 10 V, $-V_{GS}$ = 4.5 V, $-I_D$ = 1 A, R_G = 10 Ω	t_f	-	17.8	-	ns
Body-Diode PARAMETERS					
Diode Forward Voltage at $-I_S$ = 0.75 A, V_{GS} = 0 V	$-V_{SD}$	-	-	1.2	V
Diode Forward Current	$-I_S$	-	-	2.4	A
Body Diode Reverse Recovery Time at I_F = 1 A, di/dt = 100 A / µs	t_{rr}	-	5.3	-	ns
Body Diode Reverse Recovery Charge at I_F = 1 A, di/dt = 100 A / µs	Q_{rr}	-	1.7	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

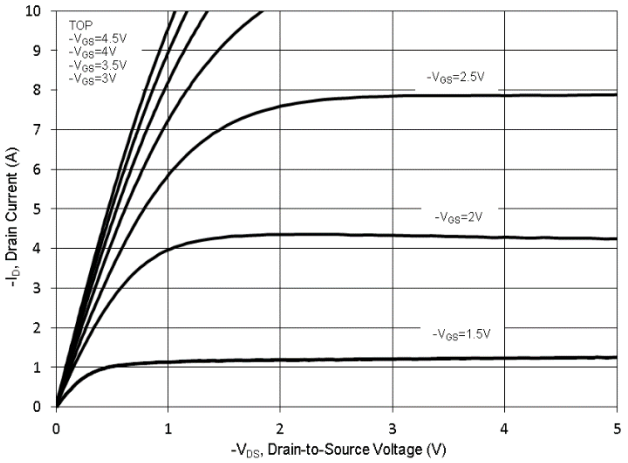


Fig. 2 Typical Transfer Characteristic

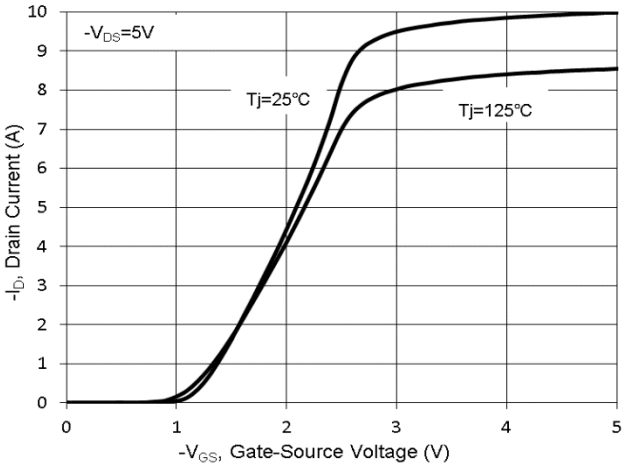


Fig. 3 on-Resistance vs. Gate Voltage

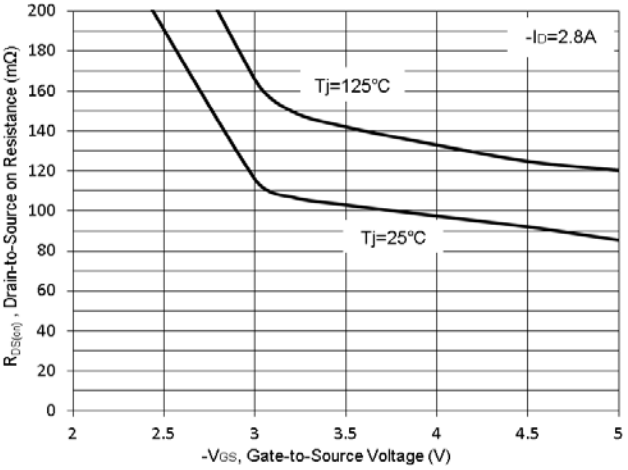


Fig. 4 on-Resistance vs.T_j

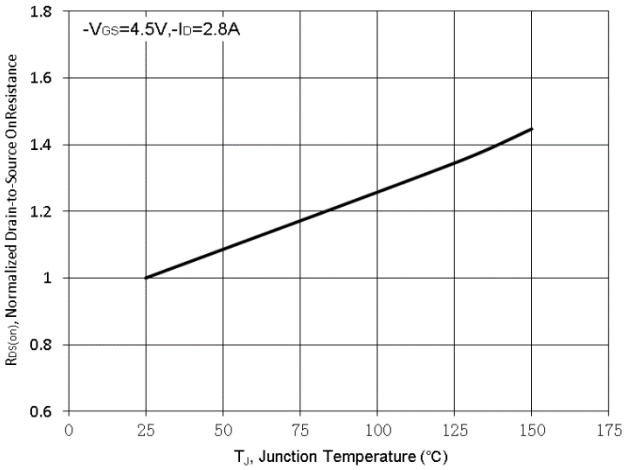


Fig. 5 Drain Current vs. on-Resistance

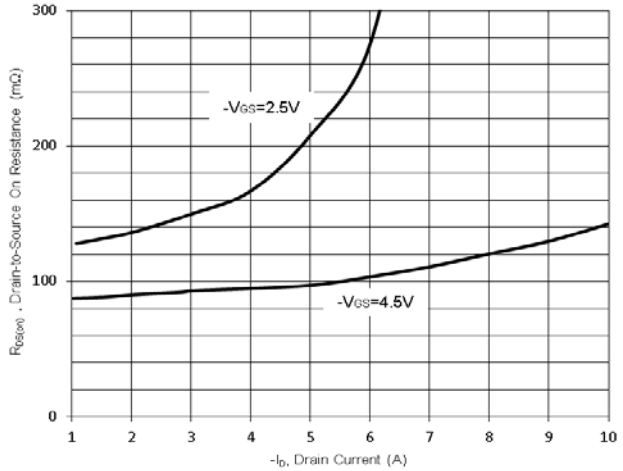
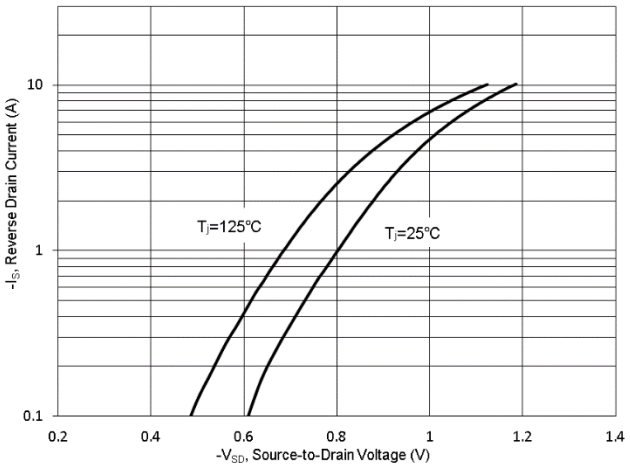


Fig. 6 Typical Forward Characteristic



Electrical Characteristics Curves

Fig. 7 $V_{(BR)DSS}$ vs. Junction Temperature

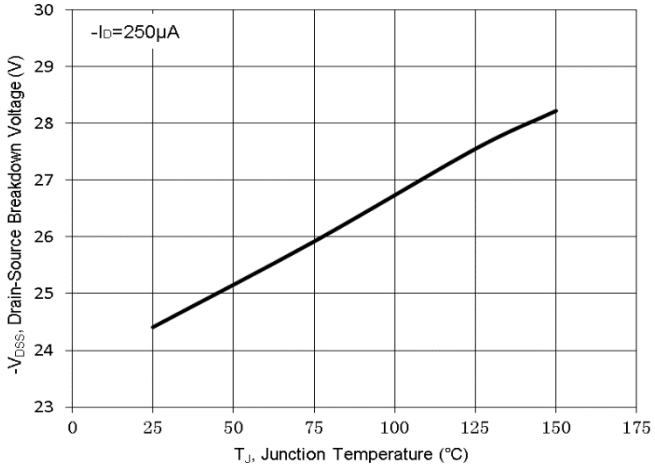


Fig. 8 Gate Threshold Variation vs. T_j

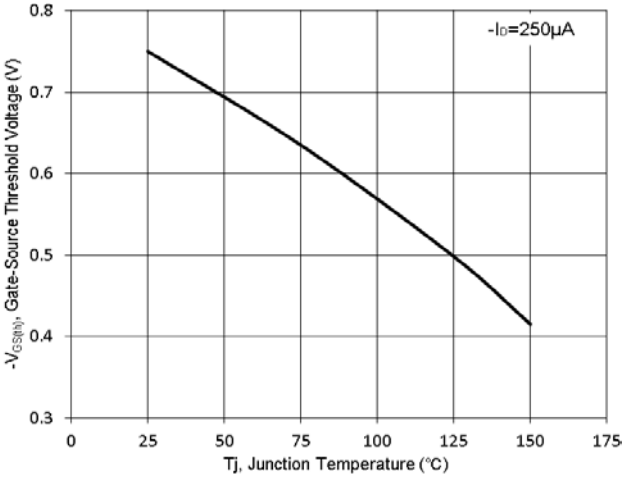


Fig. 9 Typical Junction Capacitance

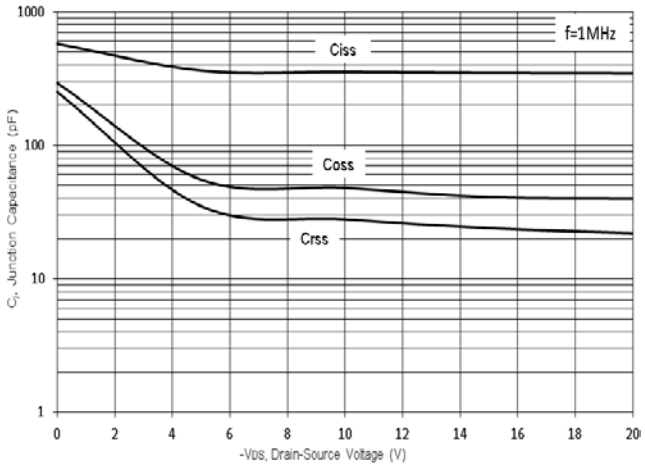


Fig. 10 Gate Charge

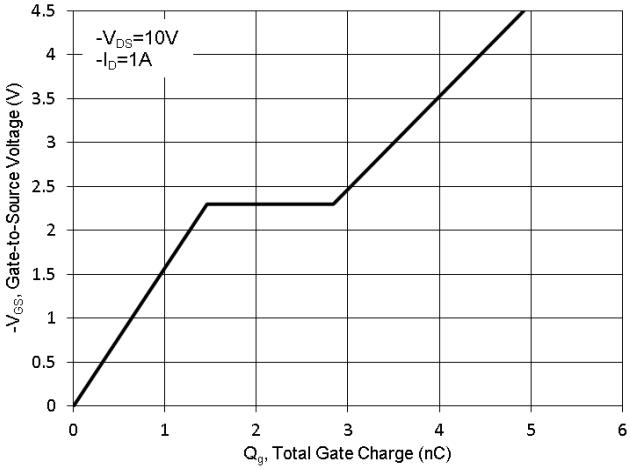


Fig. 11 Drain-Source Leakage Current

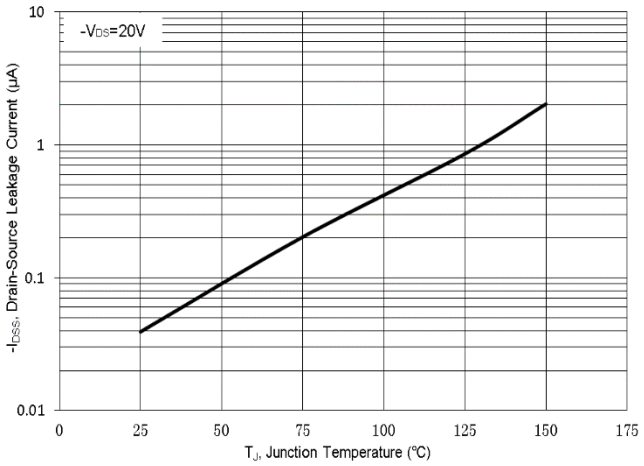


Fig. 12 Safe Operation Area

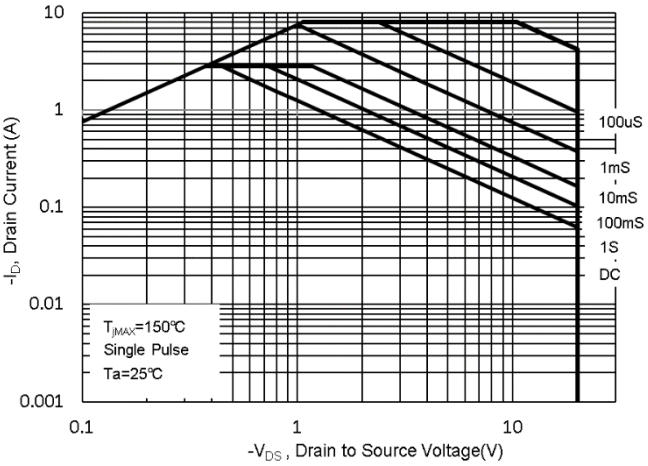
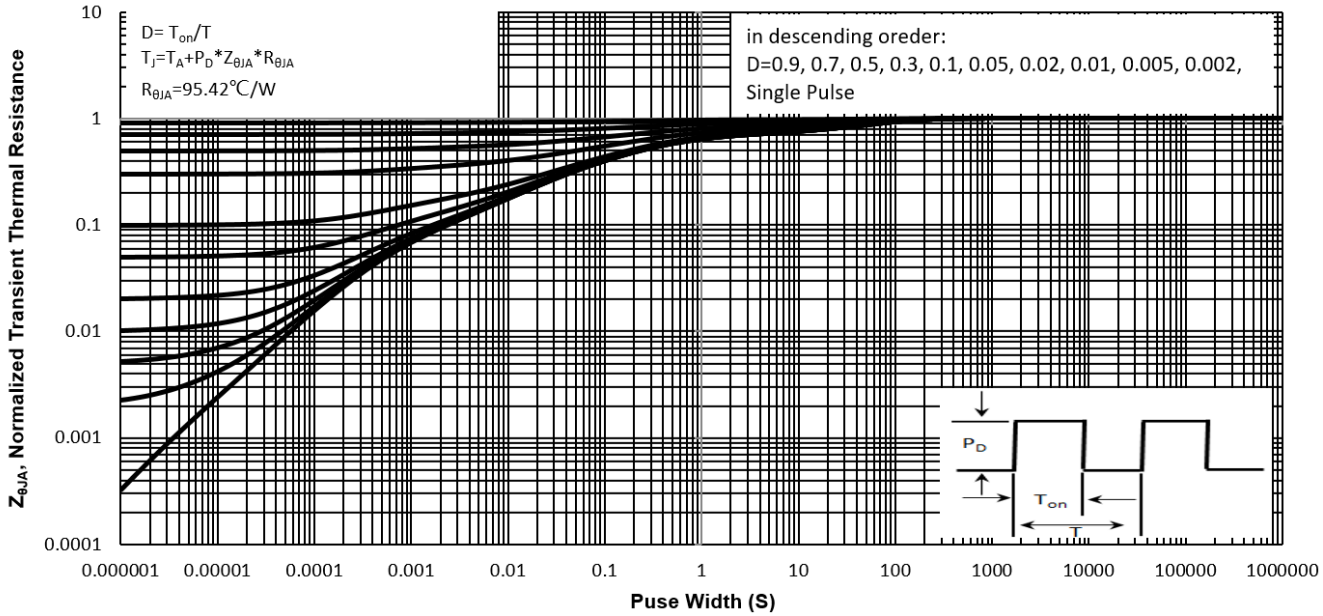


Fig. 13 Transient Thermal Resistance



Test Circuits

Fig.1-1 Switching times test circuit

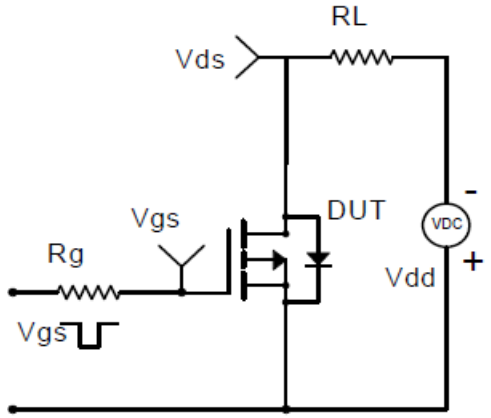


Fig.1-2 Switching Waveform

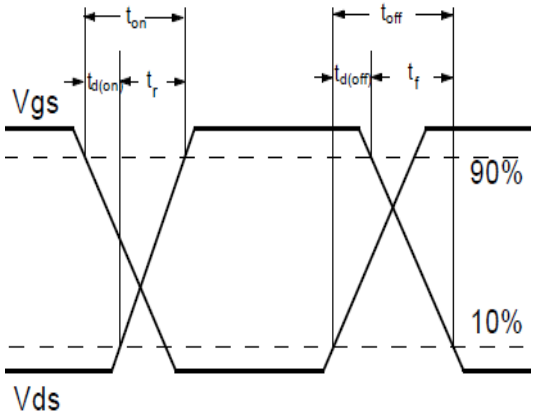


Fig.2-1 Gate charge test circuit

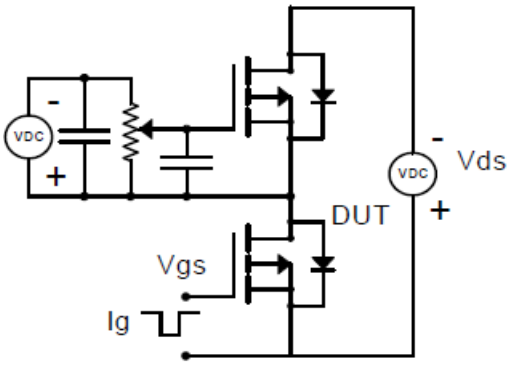
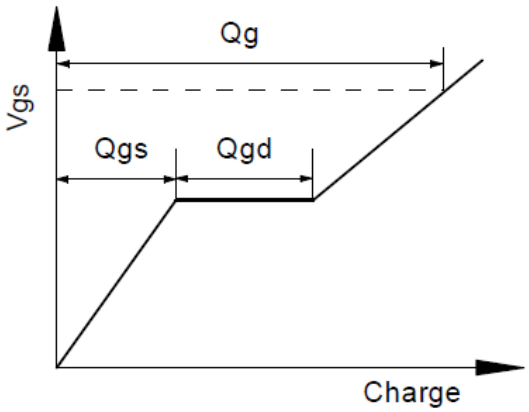
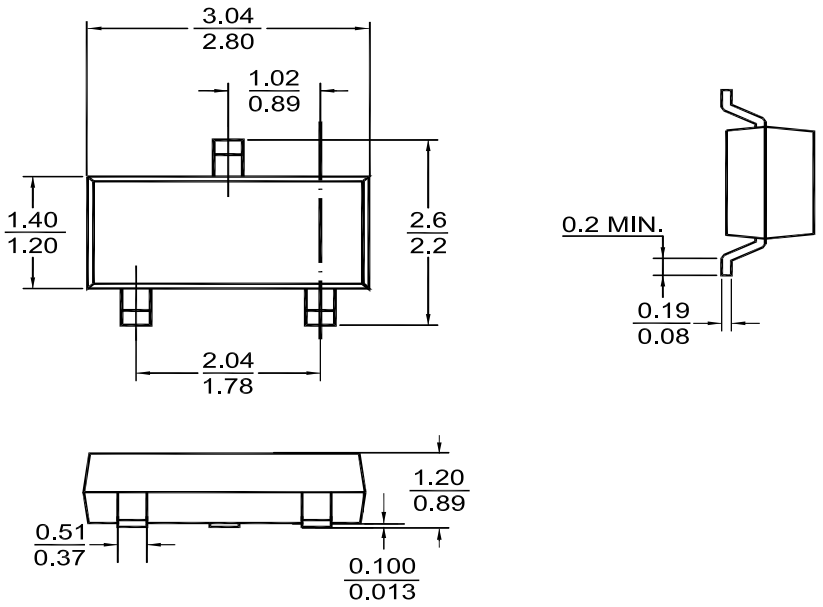


Fig.2-2 Gate charge waveform

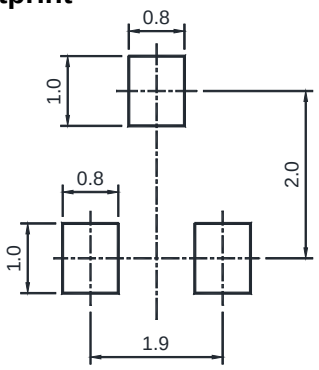


PACKAGE OUTLINE

Plastic surface mounted package (Dimensions in mm) TO-236



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
TO-236	8	4 ± 0.1	0.157 ± 0.004	178	7	3,000

Marking information

" M01 " = Part No.
"YM" = Date Code Marking
"Y" = Year
"M" = Month
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