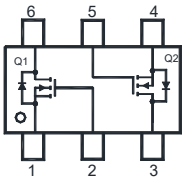
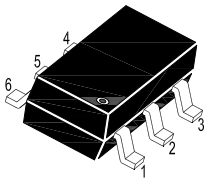
MMBT7002DW-AH

Dual N-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 Qualified
- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switching
- High saturation current capability
- High speed switching
- Halogen and Antimony Free(HAF), RoHS compliant





Q1: 1.Source 2. Gate 6. Drain
Q2: 3. Drain 4. Source 5. Gate
SOT-363 Plastic Package

Absolute Maximum Ratings (T_a = 25℃)

Parameter		Symbol	Value	Unit
Drain Source Voltage		V_{DSS}	60	V
Drain Gate Voltage (R_{GS} ≦ 1 MΩ)		V_{DGR}	60	V
Gate Source Voltage	Continuous Pulsed	V_{GSS}	± 20 ± 40	V
Drain Current - Continuous		I_D	115	mA
Peak Drain Current, Pulsed [1)]		I_{DM}	800	mA
Total Power Dissipation		P_{tot}	200	mW
Operating and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Ambient [2)]	$R_{\theta JA}$	625	℃/W

[1)] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%,Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

[2)] Device mounted on FR-4 substrate PC board, with minimum recommended pad layout.

Dated: 15/10/2020 Rev: 01

Characteristics at T_a = 25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain Source Breakdown Voltage at I_D = 10 μA	BV_{DSS}	60	-	-	V
Zero Gate Voltage Drain Current at V_{DS} = 60 V	I_{DSS}	-	-	1	μA
Gate Source Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 100	nA
Gate Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 μA	$V_{GS(th)}$	1	-	2.5	V
Static Drain Source On Resistance at V_{GS} = 10 V, I_D = 500 mA	$R_{DS(ON)}$	-	-	7.5	Ω
Drain Source On Voltage at V_{GS} = 5 V, I_D = 50 mA at V_{GS} = 10 V, I_D = 500 mA	$V_{DS(ON)}$	- -	- -	0.375 3.75	V
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 10 V, I_D = 200 mA	g_{FS}	80	-	-	mS
Input Capacitance at V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	22.5	50	pF
Output Capacitance at V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	9	25	pF
Reverse Transfer Capacitance at V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	7.5	10	pF
Total Gate Charge at V_{DS} = 30 V, I_D = 0.2 A , V_{GS} = 10 V	Q_g	-	1.08	-	nC
Gate Source Charge at V_{DS} = 30 V, I_D = 0.2 A , V_{GS} = 10 V	Q_{gs}	-	0.28	-	nC
Gate Drain Charge at V_{DS} = 30 V, I_D = 0.2 A , V_{GS} = 10 V	Q_{gd}	-	0.09	-	nC
Turn On Time at V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A, V_{GS} = 10 V, R_{GEN} = 25 Ω	$t_{d(on)}$	-	2.7	-	ns
Turn-On Rise Time at V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A, V_{GS} = 10 V, R_{GEN} = 25 Ω	t_r	-	17	-	ns
Turn Off Time at V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A, V_{GS} = 10 V, R_{GEN} = 25 Ω	$t_{d(off)}$	-	8.5	-	ns
Turn-Off Fall Time at V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A, V_{GS} = 10 V, R_{GEN} = 25 Ω	t_f	-	28	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at V_{GS} = 0 V, I_S = 0.5 A	V_{SD}	-	-	1.2	V

Electrical Characteristics Curves

Fig. 1 Output Characteristic

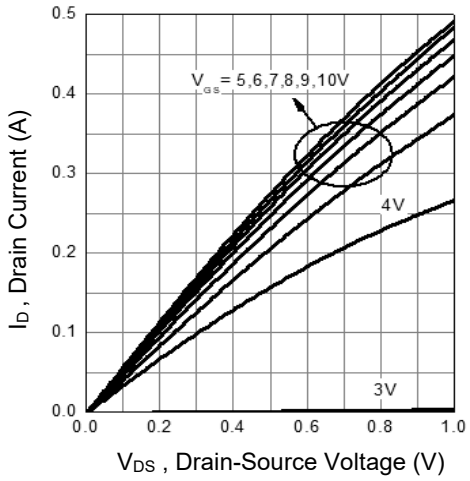


Fig. 2 Transfer Characteristics

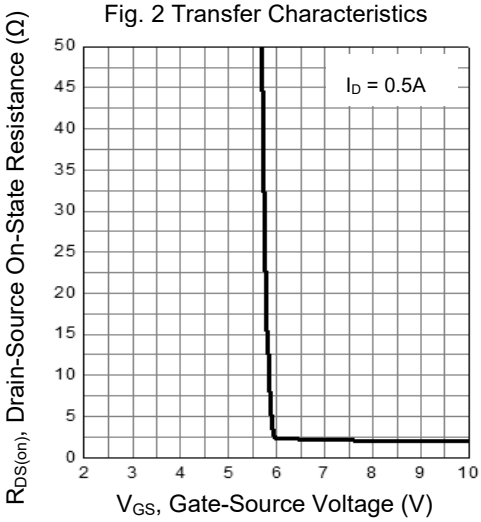


Fig. 3 on-Resistance vs. Drain Current

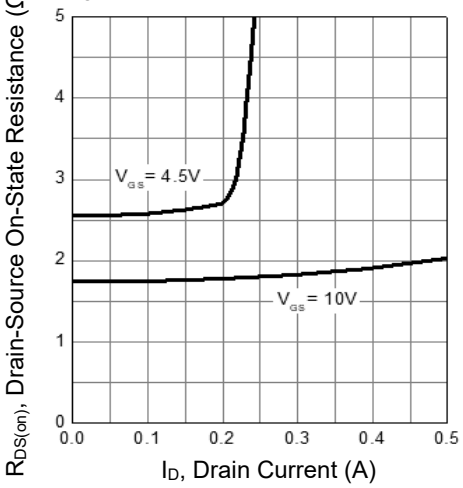


Fig. 4 Body Diode Forward Characteristic

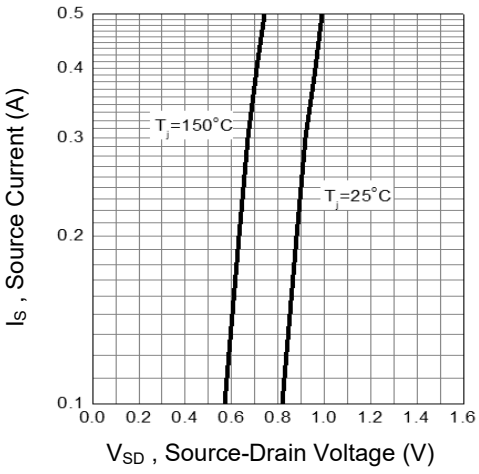


Fig. 5 $R_{DS(on)}$ vs. T_j

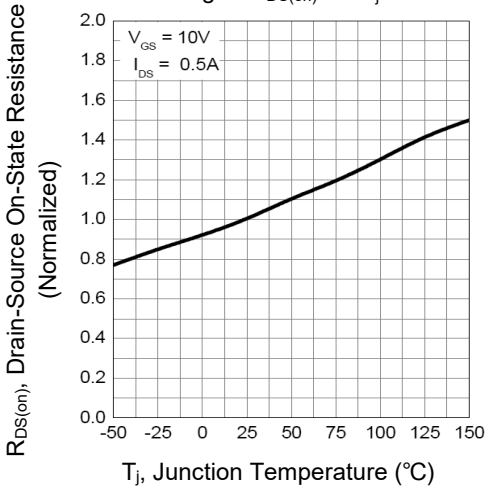
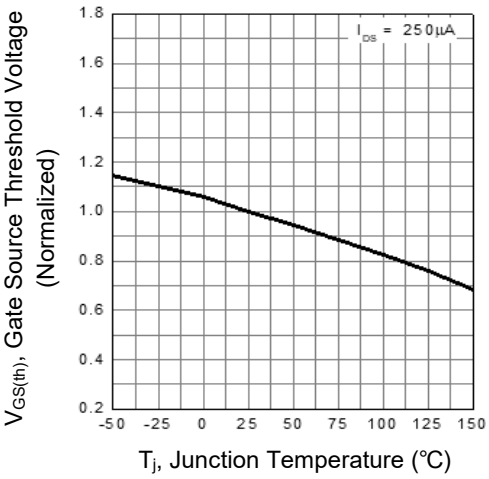


Fig. 6 $V_{GS(th)}$ vs T_j



Electrical characteristic curve

Fig. 7 Capacitance

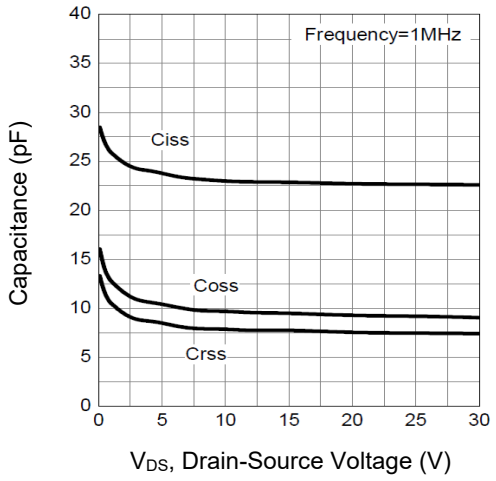
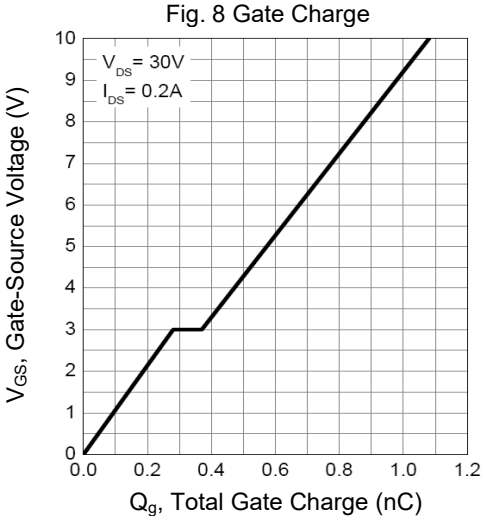


Fig. 8 Gate Charge



Test Circuits

Fig.1-1 Switching times test circuit

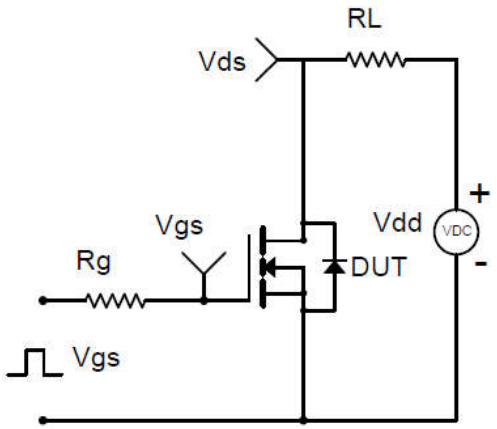


Fig.1-2 Switching Waveform

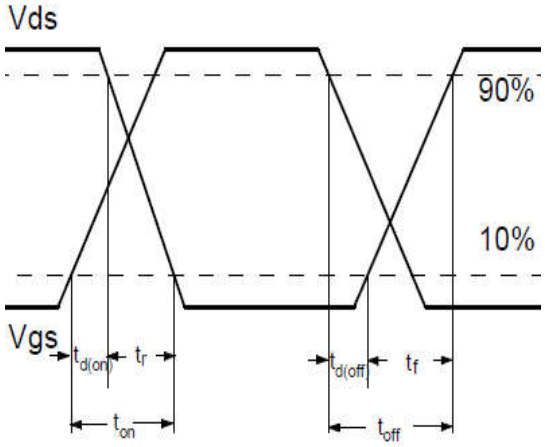


Fig.2-1 Gate charge test circuit

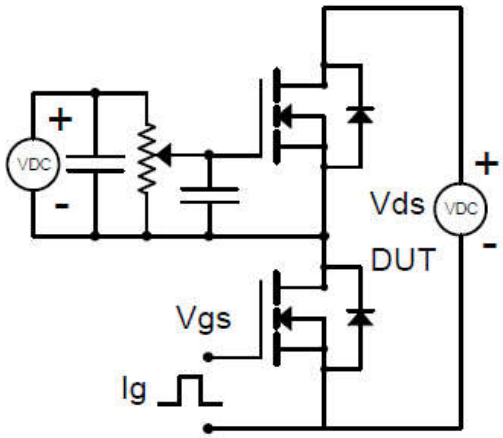
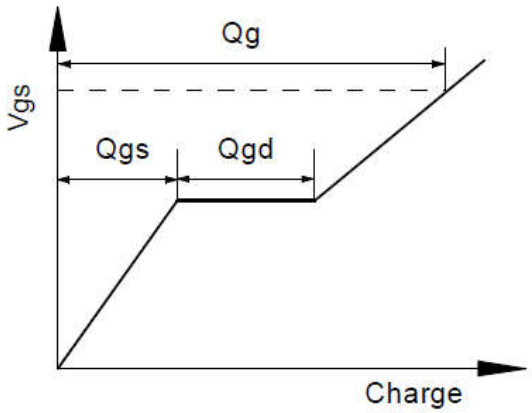
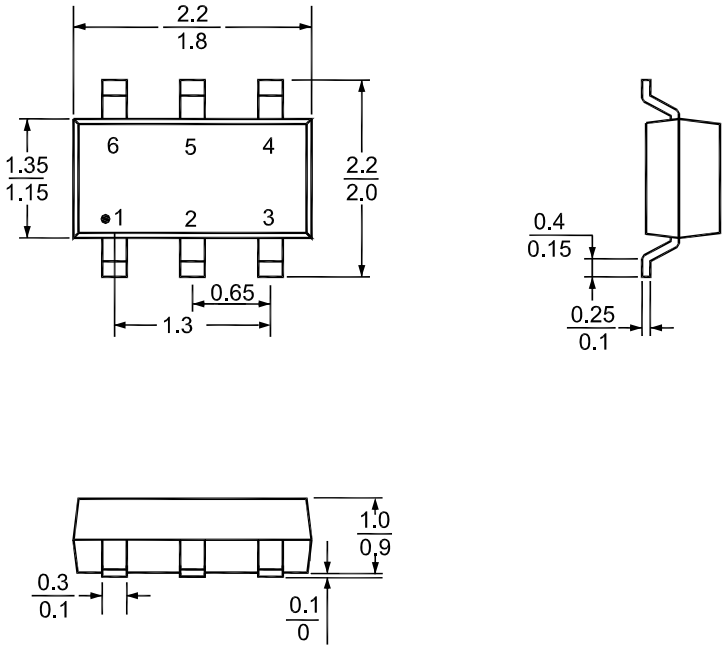


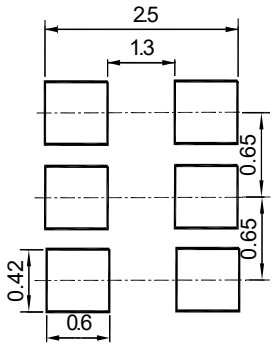
Fig.2-2 Gate charge waveform



Package Outline Dimensions (Units: mm) SOT-363



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-363	8	4 ± 0.1	0.157 ± 0.004	178	7	3,000

Marking information

" K72 " = Part No.
" • "= HAF (Halogen and Antimony Free(HAF).
"YM" = Date Code Marking
"Y" = Year
"M" = Month
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